박 사 학 위 논 문

실리콘 기반 무선통신 및 센싱용
RF 송수신기 전단부 설계연구

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Dissertation for the degree of Doctor of Engineering

Silicon-based RF Transceiver front-end Designs for Wireless Communication and Sensing Applications

Advisor: Professor Jung-Dong Park

Hyohyun Nam

Department of Electrical and Electronic Engineering

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이 논문을 박사학위 논문으로 제출함

2020 년 6 월

남효현의 공학 박사학위 논문을 인준함

2020 년 7 월

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by

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Date of submission : 2020/06
Date of approval : 2020/07

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2020

ACKNOWLEDGEMENTS

First of all, I would like to thank my advisor, professor Jung-Dong Park, for his guidance and encouragement during my study at Dongguk University. Due to his in-depth experience and visionary ideas, I have acquired the fundamental of RF integrated circuit design. I am extremely grateful for his kind technological and personal assistance and guidance in making the work possible.

I would also like to thank professor Min-Sung Kim, professor Changhwan Shin, and professor Jaeduk Han for agreeing to be on my dissertation committee, and professor Han Ho Choi for serving as the chair of my committee. Their comments and feedbacks have kept me on the right track.

I would like to thank MEIC Lab. members, Van-Son, Jeong-Moon, Van-Viet, Young Joe, Chen, Tae-Wha, Hyeon-Seok, Jun-Hee, Van-Du, and Hyeon-Hee. It was a pleasure to work with them as a lab member.

Last and most importantly, none of this would have been possible without support, motivation, patience and affection from my family and wife Hyejun Moon. This study would never have come to be without them.

ABSTRACT

Owing to the rapid development of wireless communication and sensing technology, it is necessary to design a transceiver which is compatible with existing system as well as new system standards in a single chip with various functions. The design of transceivers with the state-of-the-arts performance in communication and sensing applications should satisfy numerous types of the required specifications such as broadband operation, high linearity, miniaturization, low power consumption, and low cost. Recently, due to the aggressive development of silicon (i.e., CMOS and SiGe BiCMOS) process technology, it is possible to design silicon-based RF-front-end transceivers with comparable performances with those in III-V compound semiconductor technologies. In addition, the device models in silicon-based process are more accurate and stable compared with those used for the III-V devices. Therefore, the silicon-based integrated circuits are more advantageous for low cost and mass production. This thesis deals with various design approaches of the silicon-based RF transceivers for high-performance wireless communication and sensing applications. This thesis consists with six chapters, each of which deals independent topics as below:

Chapter 1: A brief introduction to the advantage of silicon based process technology to support both micro- and millimeter-wave designs is discussed. And then, several examples of emerging micro- and millimeter-wave applications in sensing and communications are demonstrated.

Chapter 2: An ultra-wideband low noise amplifier (LNA) is implemented in 65 nm CMOS. A compact inter-stage network utilizing one transformer and a de-Q-ing resistor for achievement of ultra-wide bandwidth is presented. The designed LNA achieves an input 1-dB compression point (IP_{1dB}) of -21.43 dBm, maximum power gain of 18.21 dB over an ultra-wideband of 1 - 13 GHz, the measured minimum noise figure (NF) of 5.28 dB and. The realized LNA occupies 0.52 mm^2 of the active area excluding pads, and it consumes 14.92 mW from 1.2 V power supply.

Chapter 3: A compact in-phase/quadrature (I/Q) up-conversion chain with high linearity is implemented in 65nm CMOS for an integrated transceiver for 5G mobile communications. The upconverter consists of 10 ~ 11.5 GHz up-conversion chains, a quadrature signal generator (QSG) based on the two coupled current-mode logic latches, and inverting amplifiers to provide the rail-to-rail local oscillator (LO) swing with a 25% duty cycle for I/Q mixers which has 46.9dB of image rejection ratio. In order to improve the output third-order intercept point (OIP3), a cross-coupled pair operating at weak inversion was used at the output of the upconverter. The upconverter achieved an OIP3 of 14.45dBm and a transmitter gain of 9.12dB. The realized I/Q upconverter with the QSG draws 48.7mW under a 1V supply, and chip area is only 0.57mm^2 including pads.

Chapter 4: An integrated 2–18 GHz four-channel compressed sensing receiver (CSRX), which performs a 128.5 × sub-Nyquist acquisition with 36-Gb/s pseudo-random bit sequence (PRBS) generators is implemented in 0.13-μm BiCMOS. The integrated four-channel CSRX includes broadband receiver chains, each of which includes a distributed RF buffer that operates as an active balun at 2–18 GHz, followed by a double-balanced passive mixer for high local-oscillator (LO)-to-intermediate frequency (IF) isolation at the IF band, and a 700-MHz variable gain amplifier. In order to perform the compressed sensing by mixing the PRBS signal as the random modulator, four independent 36-Gb/s PRBS generators are integrated. So as to sufficiently deliver the generated wideband PRBS signal to the mixer, a shunt-shunt feedback amplifier is used by the LO driver to compensate for the high-frequency loss of the PRBS LO tones during the LO generation stage. The chip draws 195 mA per channel with a 2.5-V supply.

Chapter 5: a phased-array transceiver chip operating in full X-band (8-12 GHz) is realized in 65-nm CMOS technology. The implemented transceiver for the transmit/receive module (TRM) includes a single pole double throw (SPDT) switch connected to the internal power amplifier (PA) and the low-noise amplifier (LNA) to serve as a duplexer, a 6-bit passive phase shifter, a 6-bit attenuator, and a bi-directional gain amplifier (BDGA). For digital TRM control, a 64-bit SPI scan-chain is integrated. At the output 1-dB compression point (OP_{1dB}) of 11.84 dBm, the

transmitter reaches power gain of more than of 15 dB. In order to achieve a wideband operation of the passive phase shifter, two different resonant frequencies for the phase leading and lagging networks are assigned, and are aligned the slopes of their phase responses to have the desired phase shifts at the center frequency. The RMS amplitude error is less than 0.45 dB, and the RMS phase error is less than 5° for all attenuation and phase states between 8-12 GHz while dissipating 216 mW dc power from a 1 V power supply. The receiver achieves noise figure (NF) of less than 8.4 dB and greater than 15 dB of power gain for the entire X-band. The RMS amplitude error and the RMS phase error are less than 0.45 dB and 5°, respectively, for all control states between 8-12 GHz. The receiver draws 110 mW with a 1 V power supply. The chip area of transceiver is 4×1.88 mm^2.

Chapter 6: A compact W-band divide-by-three injection locked frequency divider (ILFD) is realized in 65-nm CMOS technology. In order to provide a wide locking range, inductive feedback is used to boost the injection current. Under the suggested method, the ILFD`s the locking range can be wider than 10% without additional power dissipation and any varactor which is more than three times the locking range compared with the reference ILFD without boosting of the current injection. With the W-band input signal power of 0dBm, the measured locking range of the proposed ILFD was from 73.9GHz to 82.5GHz. At the input frequency of 78GHz, the measured phase noise at 1MHz was -117.13dBc/Hz. The realized ILFD with the inductive feedback draws 7.88mW under a 1V supply. The core size of the ILFD is 0.22mm^2.

국문초록

무선통신 및 센싱기술의 급격한 발달로 인해 단일 칩으로 기존의 시스템과 새로운 시스템 규격간의 호환이 가능하며 다양한 기능을 제공하는 송수신기 설계가 요구되고 있다. 이러한 최신 통신 및 센싱용 송수신기 설계는 충분한 RF 성능을 보장해야 할 뿐만 아니라 광대역 동작, 고선형, 소형화, 저전력소비, 저비용등 까다로운 요구사항을 만족해야 하는 과제를 지니고 있다. 최근, 실리콘 (CMOS 및 SiGe) 공정기술의 발달로 인해 III-V 족 화합물 반도체를 기반으로 하는 고성능 RF-front-end 의 성능에 준하는 시스템 반도체 회로설계가 가능하며, 핵심 반도체 소자 모델이 정확하고 공정의 안정성 또한 높아 저비용, 양산성 등에 유리하다. 본 연구는 소형화 및 저전력을 위한 실리콘 기반의 무선통신 및 센싱용 RF 송수신기 front-end 설계에 대한 내용을 다룬다.

1 장 : 마이크로파 및 밀리미터파 설계가 적용되는 실리콘 기반 프로세스 기술의 장점에 대한 간략한 소개가 주어진다. 또한, 마이크로 및 밀리미터 파 대역의 센서 및 무선통신과 관련된 몇가지 일례를 간략히 설명한다.

2 장 : 65nm CMOS 공정을 이용하여 초광대역 저잡음 증폭기를 구현하였다. 초광대역 대역폭을 달성하기 위해 하나의 transformer 와 De-Q-ing 저항으로 구성된 inter-stage network 를 설계하였다. 설계된 LNA 는 -21.43dBm 의 입력 1-dB 압축 포인트 (IP_{1dB}), 1-13GHz 의 초 광대역에서 18.21dB 의 최대 전력 이득,

5.28dB 의 측정된 최소 잡음 지수 (NF)를 달성하였다. 구현된 LNA 는 패드를 제외한 0.52mm^2 의 칩면적을 차지하며 1.2V 전원에서 14.92mW 를 소비한다.

3 장 : 5G 이동통신용 송신기를 위해 높은 선형성을 갖춘 소형 I / Q (in-phase / quadrature) Up-conversion chain 이 65nm CMOS 공정으로 구현되었다. Upconverter 는 10 ~ 11.5GHz up-conversion chain 과 rail-to-rail LO 스윙을 제공하는 2 개의 전류 모드 로직(CML) 래치를 기반으로하는 QSG (Quadrature Signal Generator) 및 inverting 증폭기로 구성되었다. Image-rejection ratio 가 46.9dB 인 I / Q mixer 의 출력 3 차 인터셉트 포인트 (OIP3)를 개선하기 위해, weak-inversion 에서 동작하는 cross-coupled pair 가 upconverter 의 출력단에 사용되었다. 구현된 upconverter 는 14.45dBm 의 OIP3 와 9.12dB 의 송신 이득을 달성하였다. QSG 를 포함한 I/ Q upconverter 는 1V 전원에서 48.7mW 를 소비하며 칩 면적은 패드를 포함하여 0.57mm^2 이다.

4 장 : 36Gb / s PRBS (pseudo-random bit sequence) 발생기로 128.5 × 서브 나이퀴스트 수집을 수행하는 통합 2–18GHz 4 채널 압축 센싱 수신기 (CSRX)가 0.13μm BiCMOS 로 구현되었다. 통합된 4 채널 CSRX 에는 광대역 수신기 체인이 포함되어 있으며, 각각에는 2 ~ 18GHz 에서 active balun 으로 동작하는 분산형 RF 버퍼가 포함되어 있고, 높은 LO-to-IF 격리도를 위한 double-balanced passive mixer, 700MHz 의 대역폭을 갖는 IF 가변 이득 증폭기로 구성되었다. PRBS 신호를 랜덤 변조기로 사용하여 압축 센싱을 수행하기 위해, 4 개의 독립적인 36Gb/s PRBS 발생기가 설계되었다. 생성된 광대역 PRBS 신호를

mixer 에 충분히 전달하기 위해 LO driver 가 shunt-shunt feedback 증폭기로 구현되었으며, LO 생성 단계에서 PRBS LO 톤의 고주파 손실을 보상한다. 구현된 압축 센싱 수신기칩은 2.5V 전원으로 채널당 195mA 를 소비한다.

5 장 : 전체 X-대역 (8-12GHz)에서 작동하는 위상 배열 송수신기 칩이 65nm CMOS 공정으로 구현되었다. 송수신 모듈 (TRM)을 위해 구현된 송수신기는 전력 증폭기 (PA) 및 저잡음 증폭기 (LNA)에 연결된 duplexer 역할을 수행하는 SPDT (Single Pole Double Throw) 스위치, 6-bit 위상 변환기, 6-bit 감쇠기 및 양방향 이득 증폭기 (BDGA)를 포함한다. 디지털로 TRM 기능을 제어하기 위해 64-bit SPI 스캔 체인이 통합되어 있다. 위상 변환기의 광대역 동작을 달성하기 위해, 진상 (Leading) 및 지상 (Lagging) 네트워크에 대한 2 개의 상이한 공진 주파수가 할당되고, 중심 주파수에서 원하는 위상 시프트를 갖도록 위상 응답의 기울기를 보정하였다. 송신기는 1V 전원에서 216mW 를 소비하며, 11.84dBm 의 출력 1dB 압축 지점 (OP1dB)에서 15dB 이상의 전력 이득을 갖는다. 또한, 8-12GHz 사이의 모든 감쇠 및 위상 상태에 대해 0.45dB 미만의 RMS 진폭 오류, 5° 미만의 RMS 위상 오류를 달성하였다. 수신기는 1V 전원으로 110mW 를 소비하며, 8.4dB 미만의 잡음 지수 및 15dB 이상의 전력 이득을 갖는다. 또한, 8-12GHz 사이의 모든 감쇠 및 위상 상태에 대해 RMS 진폭 오류 및 RMS 위상 오류는 각각 0.45dB 및 5° 미만이다. 송수신기의 칩 면적은 $4 \times 1.88\ mm^2$ 이다.

6 장 : W-대역 injection-locked 기반의 3 분주 주파수 분배기가 65nm CMOS 공정으로 구현되었다. 주파수 분배기의 locking range 를 wide 하게 구현하기 위해 주입 전류를 높이기 위한 inductive feedback 을 사용하였다. 제안된 방법 하에서 주파수 분배기의 locking range 는 추가적인 전력 손실 및 주파수 변경을 위한 varactor 없이 기존 주파수 분배기에 비해 3 배 이상 향상되었다. W-대역 입력 신호 전력이 0dBm 인 경우, 제안된 주파수 분배기의 측정된 locking range 는 73.9GHz 에서 82.5GHz 이다. 78GHz 의 입력 주파수에서 측정된 위상 노이즈는 1MHz offset 에서 -117.13dBc / Hz 이다. Inductive feedback 을 사용한 주파수 분배기의 코어 크기는 0.22mm^2 이며 1V 전원에서 7.88mW 를 소비한다.

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I. Introduction

1.1. Motivation and Background

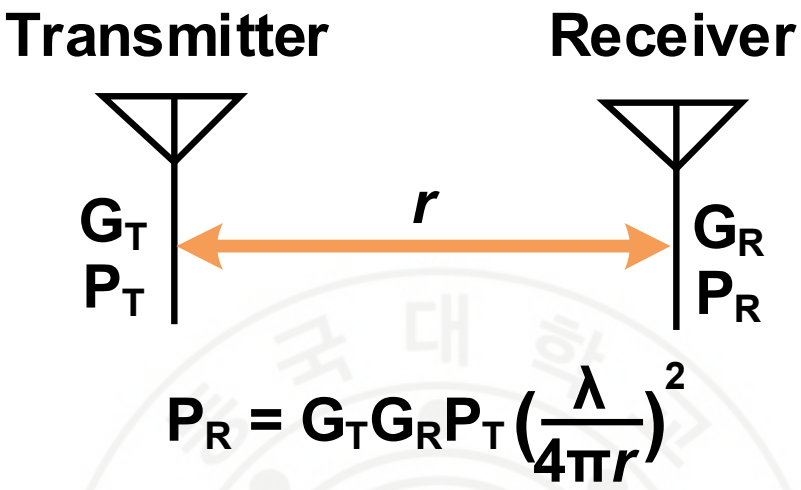


Figure I-1. Friis transmission equation [1]. λ = Wave-length(m), *r* = Distance (m), P_T = Transmitted power (W), G_T = Antenna gain for transmitter, P_R = Received power (W), G_R = Antenna gain for receiver.

In the past decades, wireless communication and sensing systems have been made rapid progress with the steadily increasing the use of frequency bands for much faster and larger data transfers. Especially, the demand for extremely high-frequency (micro-wave and mm-wave) transceivers in the systems is exploding. Here, micro-wave and mm-wave spectrums classified as extremely high-frequency are defined as 1-30 GHz and 30-300 GHz, respectively. However, the system with high-frequency propagation cannot avoid high path-loss in a transmit/receive channel path. To be more specific, the Friis transmission equation [1] used to relate the received power (P_R) and transmitted power (P_T) in the channel should be considered to successfully implement the systems, as shown in Figure I-1.

In addition, the absorb by rain, fog, and moisture for micro- and mm-waves in the air can reduce the data transmission distance resulting in signal attenuation. For example, the signal attenuation by Oxygen (O_2) absorption is extremely high at 60

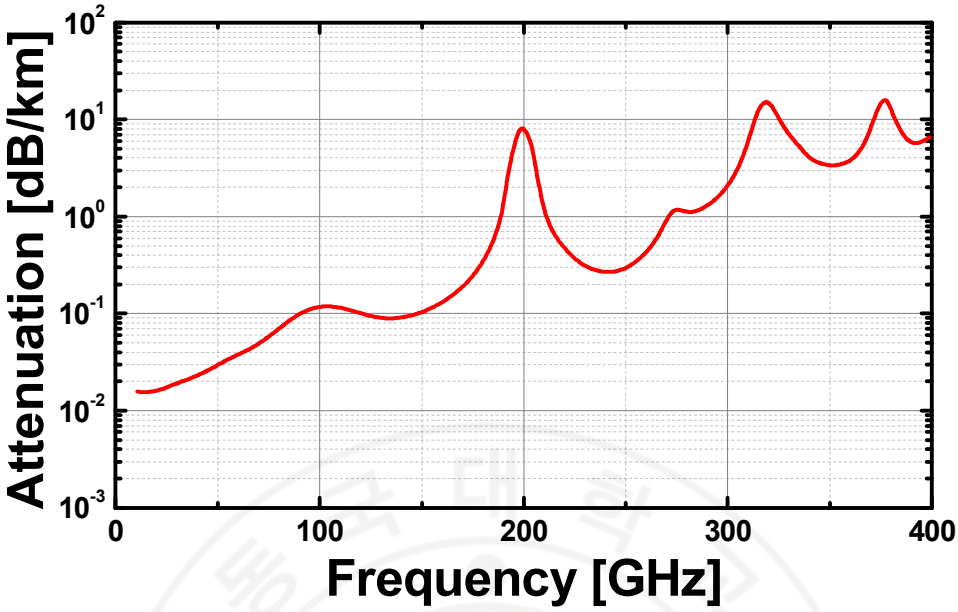


Figure I-2. Signal attenuation at sea level *versus* frequency.

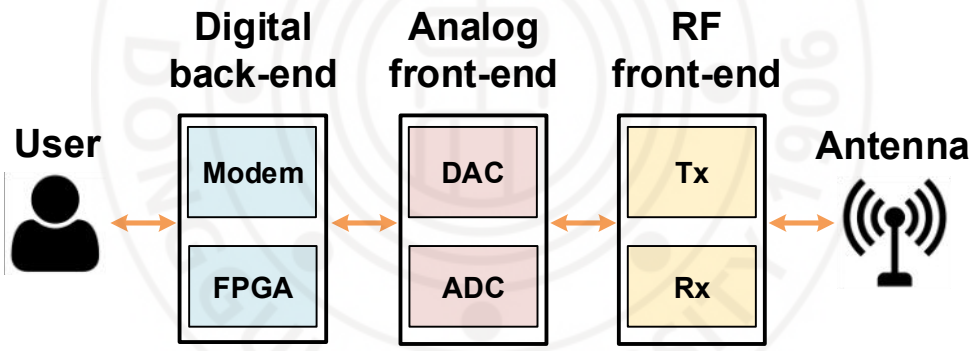


Figure I-3. The generic system overview of a point-to-point radio.

GHz as depicted in Figure I-2. Therefore, the frequency within the curve valleys in Figure I-2 should be carefully selected so as to minimize the attenuation. Additionally, a design of high-gain antenna can help with the boosted effective isotropic radiated power (EIRP) to improve the data transmission range in the systems.

Wireless products in micro-/mm-wave applications require demanding properties such as low cost, low power, high performance and large capacity. In order

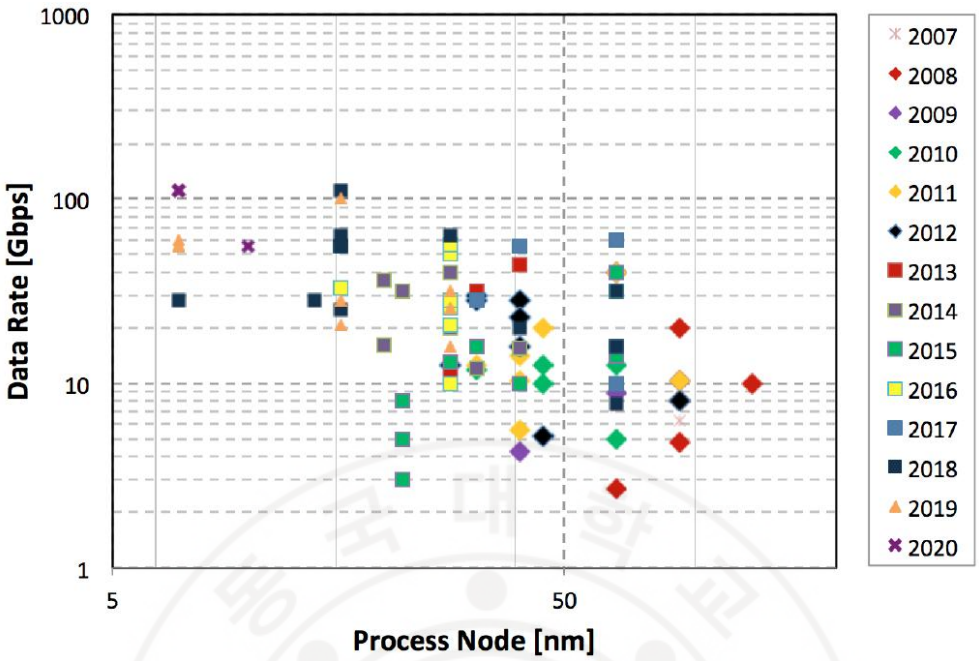


Figure I-4. Data-rate *versus* process node and year [5].

to implement the wireless communication and sensing systems, the RF-front-end is one of the key blocks in the systems as shown in Figure I-3. Historically, the systems in mm-wave applications have been dominated by III-V compound semiconductor technologies (mainly Gallium Arsenide (GaAs) and Indium Phosphide (InP)) [2-3]. However, passive elements such as inductor, capacitor, and transmission line for impedance matching and tuning are essential for the design of RF-front-end in the systems, and these elements occupy most of the chip area. Since the process cost of III-V compound semiconductor technology is quite expensive, there are limitations in implementing a fully integrated on-chip system. Therefore, the challenges are to build the RF transceiver front-end on a single chip, and to minimize the area and cost of the chip.

Recently, since the size of silicon-based transistors have steadily decreased based on Moore`s law [4], improvements in integrated circuit (IC) technology with high data rate have also been made at the same time as shown in Figure I-4 [5]. With the reduced channel length, the RF characteristics of silicon-based processes (*i.e.,* SiGe BiCMOS and CMOS) such as the cut-off frequency (f_t) and maximum

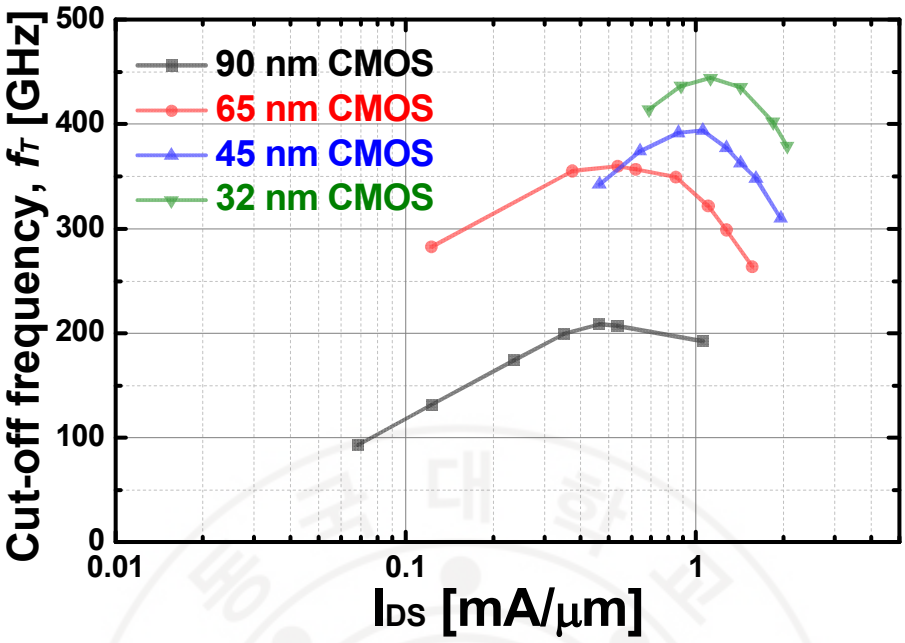


Figure I-5. Maturation of f_T in CMOS technology [6].

Company[1]	Freescale		IBM			Infineon		TowerJazz		STMicroelectronics	
Name	HiP6MW	HiP6MW2	BiCMOS8HP	BiCMOS8XP	BiCMOS9HP	B7HF200	B11HFC	SBC18H3	SBC18H4	BiCMOS9MW	BiCMOS055
Status	Prod.	Dev	Prod.	Prod?	Dev.	Prod.	Dev.	Prod.	Dev.	Prod.	Dev.
CMOS node	180nm		130nm		90nm	Bipolar-only	130nm	180nm	180nm	130nm	55nm
Wafer Size	200mm		200mm			200mm		200mm		200mm	300mm
SiGe HBT structure	Self-aligned SEG epi.		Self-aligned NSEG epi.			Self-aligned SEG epi.		Self-aligned NSEG epi.		Self-aligned SEG epi.	
SiGe HBT f_T / f_{MAX} (GHz)	200 / 280	260 / 350	210 / 270	260 / 320	300 / 350	190 / 250	240 / 380	240 / 270	275 / 350 (tbc)	220 / 280	320 / 370
BEOL (w/o Alu cap)	5 Cu levels (0.8 μm top metal)		3 Cu+2 Al levels (1.25 μm + 4.0 μm)		NA	4 Cu levels (0.6/0.6/1.2/2.5 μm)	6 Cu levels (0.29/0.32/0.32/1.0/2.8 μm)	Up to 6 Al levels with at least 1 thick top metal		6 Cu levels (0.26/0.35/0.35/0.9/3.0/3.0μm)	8 Cu levels (0.16/0.2x4/0.9/3.0μm)
TL (μ-strip)	1.25 dB/mm @ 77GHz	<1 dB/mm @ 80GHz	0.9 dB/mm @ 60GHz		NA	NA	NA	NA	NA	0.5 dB/mm @ 60GHz	0.65 dB/mm @ 50GHz

Figure I-6. Main process features of SiGe BiCMOS technology industrial manufacturers [7].

frequency of oscillation (f_{max}) was significantly improved as illustrated in Figures I-5 and 6 [6-7]. As can be seen from the Figures, the Silicon-based RF transceiver front-end can be fully integrated with the analog front-end and digital back-end on a single chip.

1.2. Applications

The following sections will illustrate some of wireless communication and sensing applications in micro- and mm-wave bands.

1.2.1. 5G Wireless communication

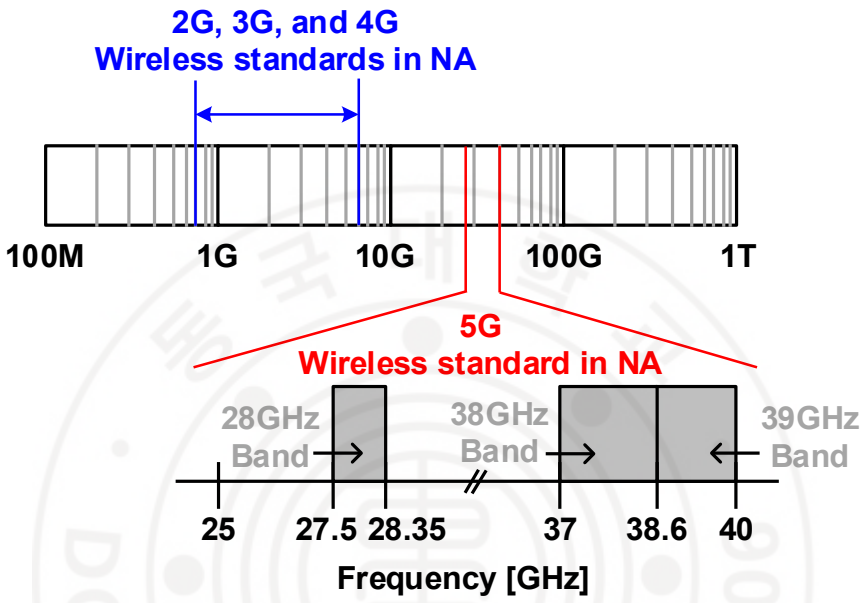


Figure I-7. The current wireless standards spectrum allocation in North America.

We are now living in a 5G era that supports massive MIMO (Multiple-Input-Multiple-Output) communication, Device-to-Device (D2D) communication, and Machine-to-Machine (M2M) communication [8-9]. Figure I-7 shows North America's current cellular wireless standard spectrum allocation for the International Telecommunications Union (ITU) radio bands scale. The limited bandwidth of the f spectrum below 6 GHz cannot meet the mobile traffic explosion in the current era. Therefore, for higher data rate and wider bandwidth, a spectrum is used in the mm-wave band for the 5G standard [10-11]. This is made possible by the advance in semiconductor technology that can build silicon-based integrated circuits (ICs) and systems-on-chips (SoCs) in mm-wave band [12]. 5G is in place in the mm-wave frequency range, and the Federal Communications Commission (FCC) recently allocated a total of 3.85 GHz bandwidth for use in the 5G standard in the 28 GHz, 38 GHz and 39 GHz bands as shown in Figure I-7 [13].

1.2.2. Compressed Sensing

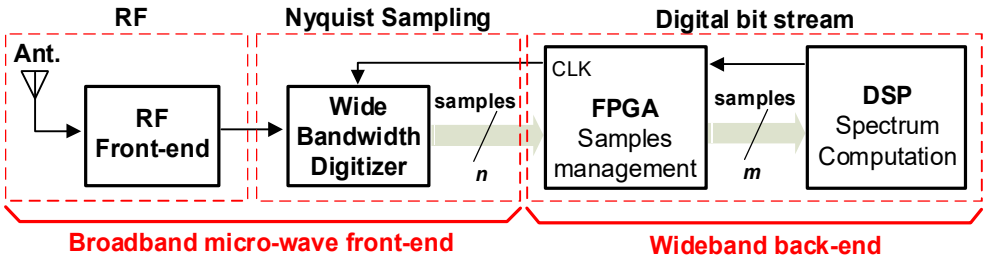


Figure I-8. Block diagram of the broadband measurement system with Nyquist sampling used for broadband signal measurement.

Figure I-8 shows the general configuration of a broadband RF signal acquisition system based on the Nyquist sampling theory [14]. The broadband signal acquisition system consists of a front-end block that receives a wideband high-frequency signal through an antenna which generates an analog signal suitable for the input of the ADC by performing amplification, filtering. The output signal of the front-end is processed for real-time digital acquisition at a high-speed back-end block. The back-end block consists of a high-speed FPGA, an ultra-high speed ADC of several tens of Gb/s, a high-speed memory, a high-speed data transmission device, and a digital signal processing (DSP) with a high computation power for processing massive digital data sets.

Nowadays with the advancement of silicon technology, 20 Gb/s or even faster interleaved ADCs with have been reported as an integrated circuit (IC) [15]. However, to process broadband signals in real-time, a multiple-interleaved architecture consisting of high-speed ADCs has to be implemented as an expensive module which consumes tens of watts of power, and its size is also considerably bulky [16]. Therefore, it is challenging to implement a receiver that collects unidentified signals at micro-wave range with Nyquist theory, especially when we want to implement a miniaturized micro-wave receiver for real-time signal acquisition with relatively low power consumption.

Recently, a compressed sensing receiver that can perform a real-time signal reconstruction has been presented as an excellent alternative to avoid aforementioned

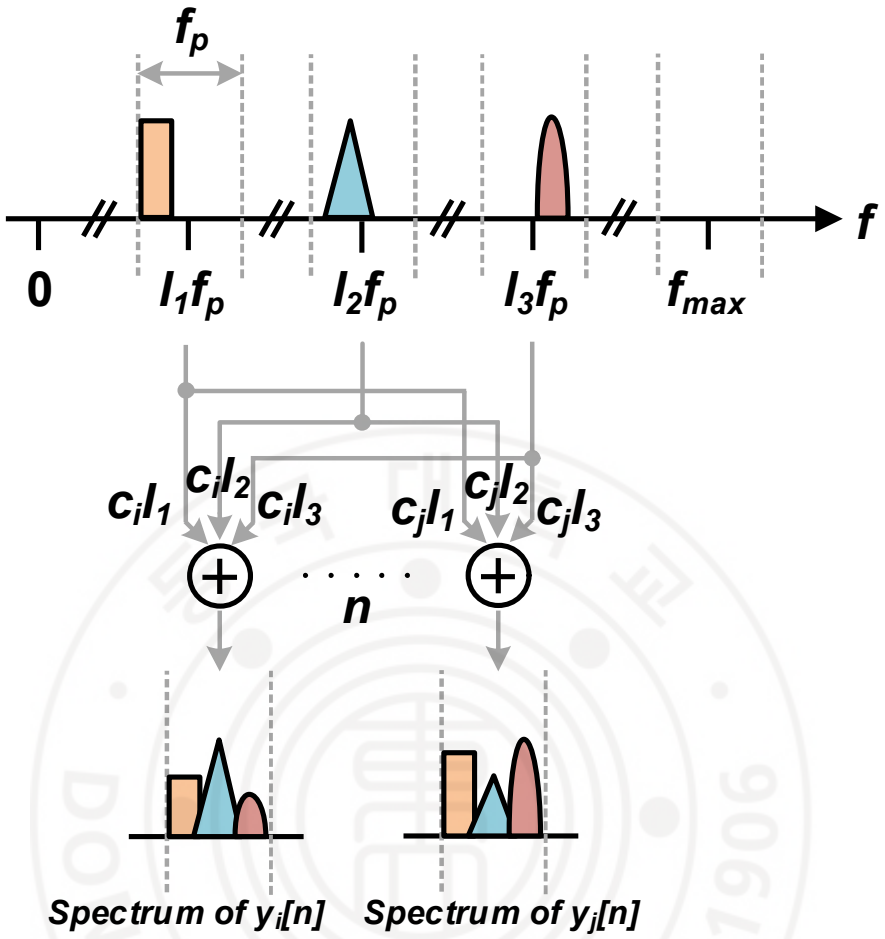


Figure I-9. The spectrum slices from x(t) are overlayed in the spectrum of the output sequences y[n].

issues. As depicted in Figure I-9, when the input signal is sparse, it has been shown that the signal reconstruction is possible even with sub-Nyquist sampling frequency by utilizing a random sensing matrix that meets the restricted isometry property (RIP) condition. This compressed sensing theory is being actively researched to speed up, optimize, and simplify signal processing systems in various fields such as wireless channel estimation in the wireless communication field, high-resolution radar signal surveillance for broadband signals, and medical image signal processing.

1.2.3. Phased-array system

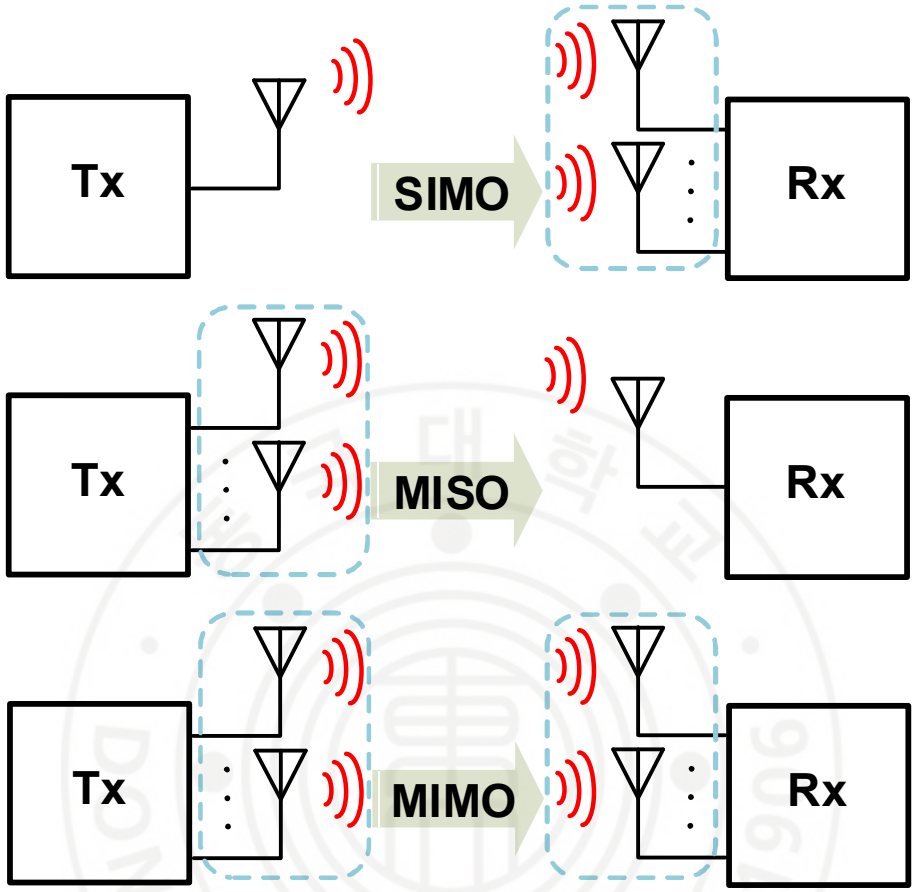


Figure I-10. Examples for multiple antenna system.

Multiple antenna system is capable of steering nulls and lobes of an antenna beam to reduce delay spread of the channel and to improve signal-to-noise ratio (SNR), by implementing beamforming. The system can be implemented on either the transmit side (multiple-input single-output: MISO), the receive side (signal-input multiple-output: SIMO), or both sides (multiple-input multiple-output: MIMO) [17] as shown in Figure I-10. Especially, the MIMO system utilizes antenna space diversity to create an independent channel path, and then, combines the received signal in an optimum way using space-time processing [18-20]. The implementation for the MIMO system based on the multiple antennas has intrigued industrial efforts and huge number of research in last decade.

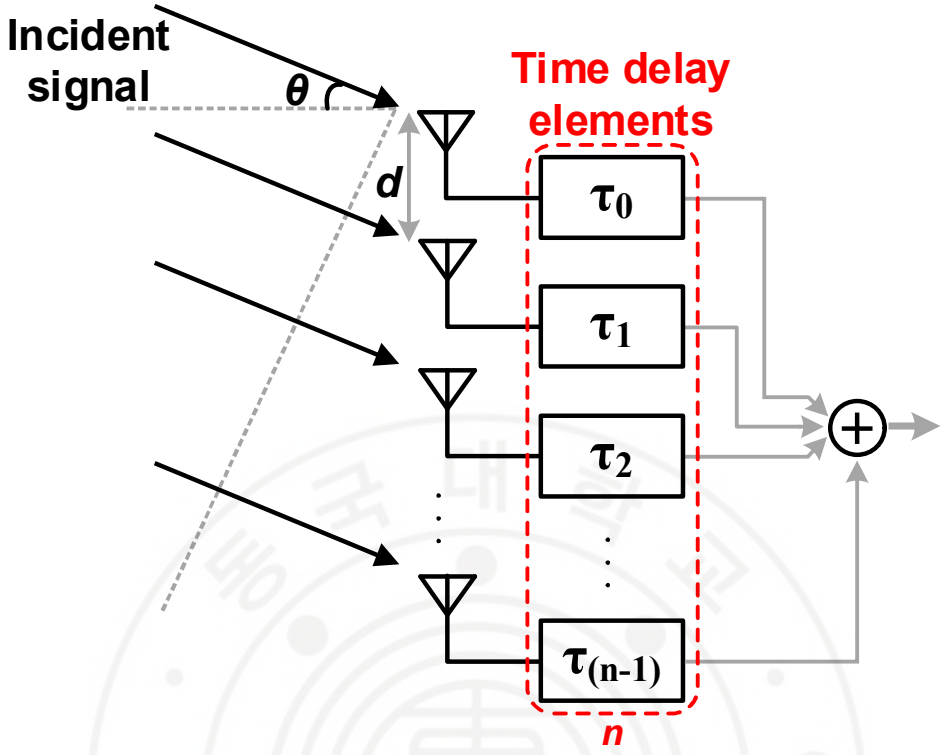


Figure I-11. A generic phased-array architecture.

Even though the multiple antenna system can be easily implemented to the base station for a wire-less mobile communication [21], the system is not suitable for mobile devices. This is because it requires the comparatively higher power according to small hardware sharing. And also, an antenna separation on the order of a magnitude, which can be higher than the wavelength, is needed to obtain a low channel correlation coefficient [22]. In order to solve these problem, the phased array system is introduced. A phased array receiver consists of independently separated signal paths, each of which is connected to separate antenna. Generally, incident signal from radiated transmitter arrives at spatially-separated antennas at different times as shown in Figure I-11. An ideal phased-array system with a time delay element such as phase shifter compensates the time delay, and combines the signals coherently to enhance the receiver sensitivity from the desired direction while rejecting receptions from other directions.

1.2.4. FMCW radar

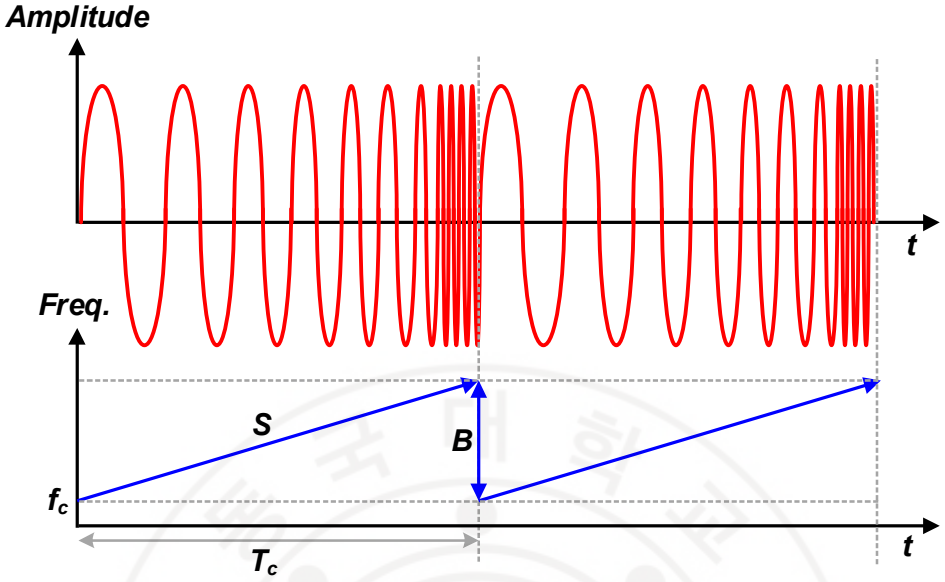


Figure I-12. Chirp Signal in the amplitude and frequency domains depending on time.

The main concept of frequency modulated continuous wave (FMCW) radar is a signal which is known as a chirp. The signal can be defined as a sinusoidal wave with a frequency value that increases linearly depending on time as shown in Figure I-12. The characteristic of the chirp signal with linear increase can create the saw-tooth type frequency like the blue-colored line in Figure I-12. As can be seen from Figure I-12, we can define four important characteristics that demonstrate the chirp signal. First of all, the frequency of f_c is the initial frequency. Secondly, the frequency sweep bandwidth of B represents the frequency interval between the start and end. Thirdly, the chirp duration of T_c represents the allocated cycle time for the chirp. Finally, the chirp slope of S represents the rate of change of the chirp signal frequency per unit of time, and can be defined as below

$$S = \frac{B}{T_C} \tag{1-1}$$

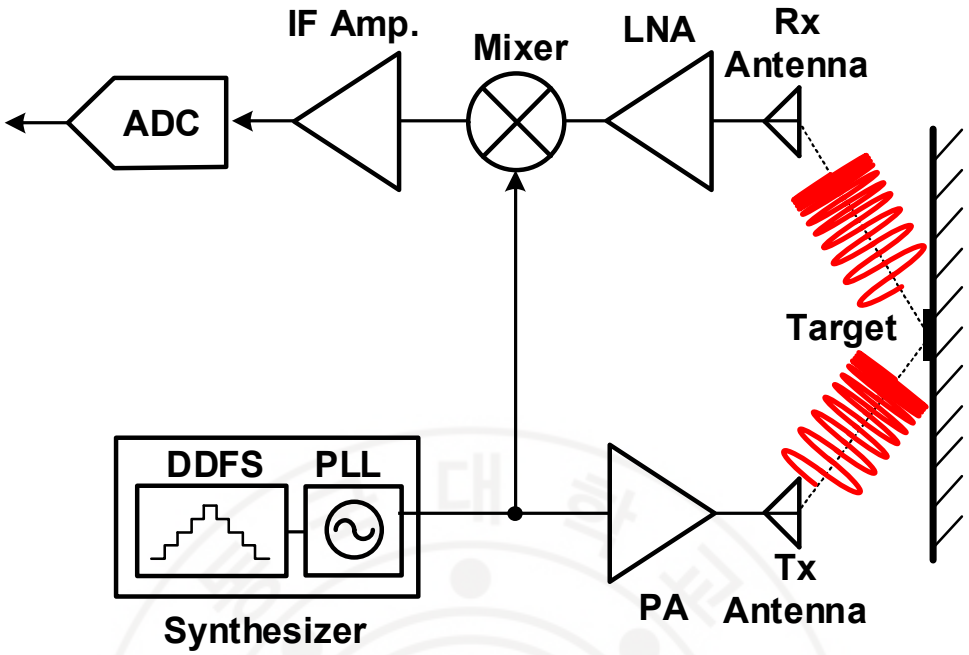


Figure I-13. The workflow diagram for the FMCW radar.

As shown in Figure I-13, the workflow diagram for the FMCW radar is presented as follows. Initially, an on-chip synthesizer (composed by DDFS and phase-locked loop) creates the chirp signal based on the different user-configurable chirp parameters. Once the chirp is amplified by a power amplifier and transmitted through Tx antenna, the Rx antenna detects the reflected and delayed chirp signal as compared with original chirp signal. The received signal is amplified by a low-noise amplifier (LNA), and then, is mixed with the original chirp signal to generate the beat frequency or IF signal. Finally, the down-converted IF signal can be amplified by an IF amplifier, and then, delivered to an ADC. The resulting serialized digital signal from the ADC can be ready to be transmitted to any other device.

1.3. Thesis Organization

In this study, the designs of RF transceiver front-end for silicon-based wireless communication and sensing applications in micro- and mm-wave bands with chip miniaturization and low power consumption are discussed.

In chapter 2, a compact wideband matching network utilizing a single transformer and a de-Q-ing resistor, where the negatively coupled transformer, is proposed so as to achieve considerable size reduction compared with the π-type inductor peaking (PIP) network.

In chapter 3, a compact I/Q upconverter as an IF up-mixer block with a bandwidth of 800MHz for a 5G wireless transceiver is presented. The upconverter with a QSG achieves high linearity by utilizing a cross-coupled pair operating at the weak inversion region to provide 3rd harmonic compensation from the GM stage for IM3 improvement. To generate I/Q signals with 25% of the duty cycle from the available $2f_{LO}$ signal, we utilized a frequency divider based on current-mode logic (CML) latches for the compact implementation of the QSG.

In chapter 4, an ultra-fast CSRX with a 128.5 × sub-Nyquist acquisition for the spectrum monitoring in the range of 2–18 GHz is described. To achieve broadband operation, we implemented broadband LO chain with a shunt-shunt feedback amplifier with equalization capability. The implementation of microwave broadband compressed sensing is achieved based on the concept of the analog-to-information converter (AIC).

In chapter 5, a fully integrated TRM chip operating in full X-band (8 – 12 GHz) is implemented in 65-nm CMOS technology. Compared with the previous work, the proposed TRM chip is designed to cover the full X-band by designing a broadband phase shifter, and a high-performance power amplifier is designed in the Tx path to achieve output power higher than 11 dBm. The implemented transceiver achieves an RMS phase error of less than 5°, and an RMS attenuation error of less than 0.45 dB with linearity and noise performance comparable to the recently reported SiGe transceiver and III-V TRM MMICs, and with much lower power consumption.

In chapter 6, a W-band divide-by-three ILFD with an inductive feedback network is proposed to enhance the injection current without any frequency tuning component like a varactor or additional power consumption in achieving a wider locking range.

In chapter 7, the research of RF transceiver front-end designs for wireless communication and sensing applications concludes.

II. 1-13 GHz CMOS low-noise amplifier using compact transformer-based inter-stage networks

2.1. Introduction

Developing exploration on ultra-wideband (UWB) frameworks has expanded enthusiasm for broadband low-noise amplifier (LNA) design. A broadband LNA must have low noise figure (NF) and good input matching over a multi-GHz bandwidth (BW) with low power dissipation. The UWB LNA ought to be deliberately intended to give an adequately enormous amount of power gain with minimum noise added to the framework. In UWB framework, LNA is required to achieve a moderate passband gain with low group delay over the passband. In addition, it should provide the wideband impedance matching to 50 Ω at the input to minimize the signal reflection at interface between a receiving antenna or band-pass filter (BPF) and the LNA input.

A multiple-section bandpass filter with inductively generated common-emitter (CE) SiGe, or common-source (CS) CMOS LNA have been proposed in [23-24] so as to achieve wideband impedance matching. As compared with the CS-LNA, the common-gate (CG) LNA proposed in [25] can reduce power consumption and improve the linearity. However, the large number of inductors increased the NF and also consumes a significant amount of chip area. Using a common gate (CG) transistor for input matching is proposed in [26-28], but the additional CS stage consumes more power and degrades the linearity. In order to achieve the capacitor cross-coupled g_m-boosting, a differential CG-LNA with stagger-compensated series-peaking technique is reported in [29]. However, the capacitor coupled g_m-boosting has slightly better noise performance, but cause potential instability though it.

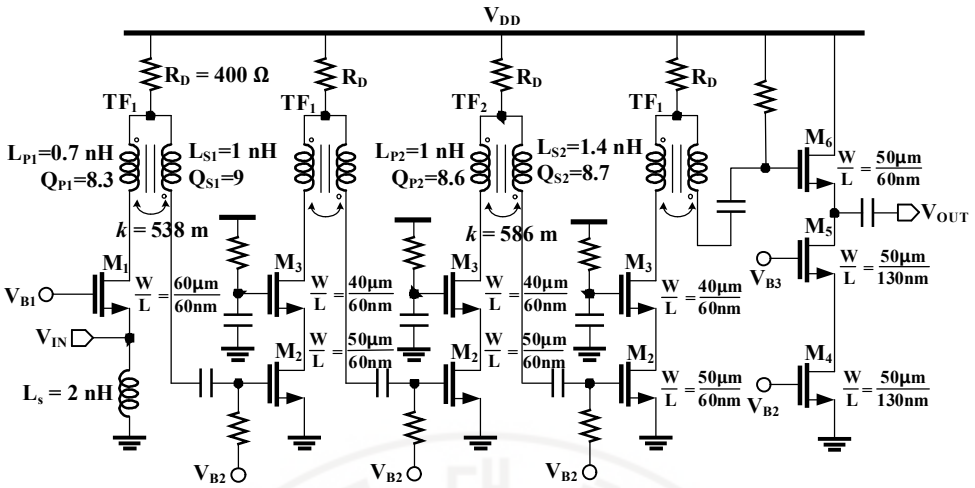


Figure II-1. Schematic diagram of the proposed wideband LNA[30].

2.2. Transformer-based UWB LNA

Figure II-1 shows a schematic diagram for the LNA. The designed LNA consists of five stages, each of inter-stage network is utilizing a de-Q-ing resistor and a single transformer for a wide bandwidth. The proposed compact transformer-based inter-stage network has comparable bandwidth enhancement ratio (BWER) as for the π-type inductor peaking (PIP) network with much smaller area consumption[30]. The designed 1-13GHz LNA is intended for an UWB radar in motion sensing and high precision-ranging applications.

A CG amplifier with a source inductor is used as the first stage to provide a wideband 50 Ω matching at the input. The source inductor is to provide the bias current and to increase the input bandwidth by resonating out the node capacitance at the center frequency while achieving a moderate NF and a good linearity. In order to achieve a wideband inter-stage network with compact area occupation, total five stages are cascaded, each of which utilizes drain and gate parasitic capacitances and a transformer with a series resistor.

After the CG stage, for a wideband output impedance matching, it has three consecutive cascode amplifiers followed by the source follower at the output stage. With a desired bandwidth of 1 - 13 GHz each transformer`s self-resonance frequency

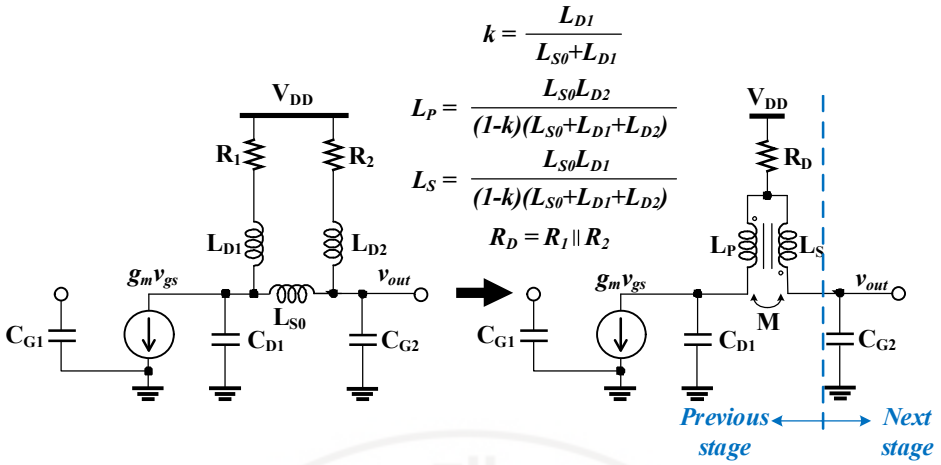


Figure II-2. The small-signal equivalent circuit models for a conventional cascaded CS amplifier with a π-type inductor peaking technique [31] and the proposed inter-stage network based on a single transformer.

should be higher than the highest operating frequency to ensure stable operation of the circuit.

In [31], π-type inductor peaking (PIP) approach is proposed to achieve BWER greater than 3. Although PIP can greatly increase the bandwidth of the cascaded amplifier, three separate inductors (L_{D1}, L_{D2}, and L_{S0} in Figure II-2) and two resistors (R_1 and R_2 in Figure II-2) are required for each inter-stage of the cascaded amplifiers, rendering the multistage amplifier quite bulky. This massive PIP can be effectively approximated into a single compact transformer with a small resistor as shown in Figure II-2. The trans-impedance transfer-function $Z_{TF}(s)$ for an inter-stage network based on a negatively coupled transformer is derived as follows:

$$Z_{TF}(s) = \frac{v_{out}}{-g_m v_{gs}} = -\frac{sM - R_D}{1 + sA_0 + s^2 A_1 + s^3 A_2 + s^4 A_3} \quad (2\text{-}1)$$

where

$$
\begin{aligned}
M &= k\sqrt{L_P L_S} \\
A_0 &= R_D(C_{G2} + C_D) \\
A_1 &= C_D L_P + C_{G2} L_S \\
A_2 &= C_D C_{G2} R_D (L_P + L_P + 2M) \\
A_3 &= C_D C_{G2} L_P L_S (1 - k^2)
\end{aligned}
\tag{2-2}
$$

Through using the proposed inter-stage network based on transformer as a compact wideband matching network, BWER is comparable to PIP approach with far smaller occupancy area. The ultra-thick metal (UTM) with the thickness of 3 μm is used to minimize the ohmic loss for the transformer windings. The designed TF_1 and TF_2 occupy an area of 200 x 200 μm^2 and 245 x 245 μm^2, respectively.

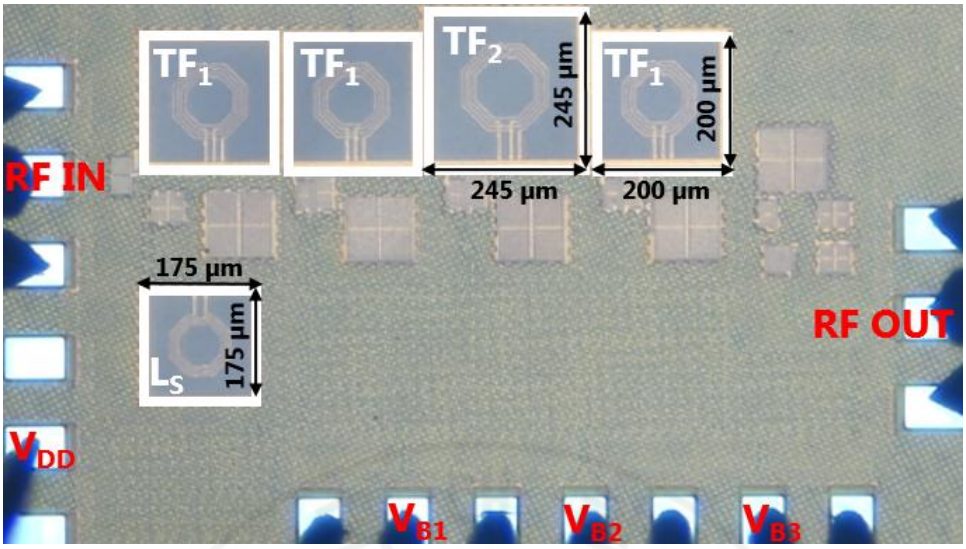


Figure II-3. Chip photograph of the LNA (Size : 0.43 x 1.20 mm^2 including pads).

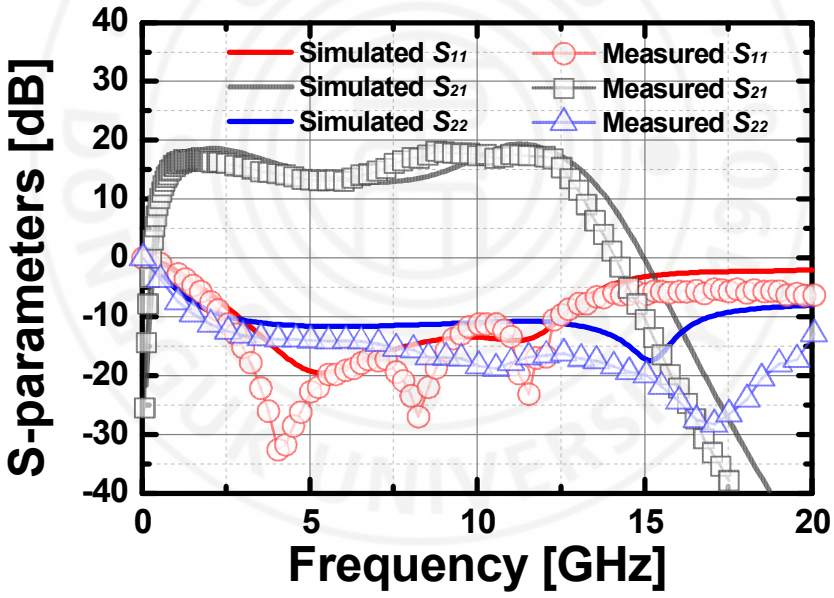


Figure II-4. Measured and simulated results of S-parameters for the LNA.

2.3. Measurement results

The proposed LNA was implemented with 65 nm RF-CMOS. As shown in Figure II-3, the overall chip area for the UWB LNA is 0.43 x 1.20 mm^2. The power consumption of the LNA is 14.92 mW from a 1.2 V supply.

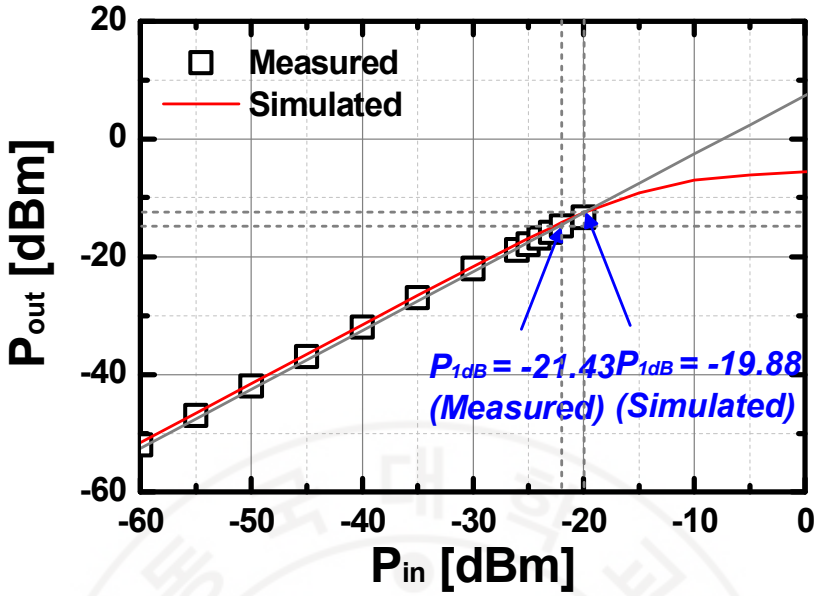


Figure II-5. Measured and simulated results of P1dB for the LNA at 6 GHz.

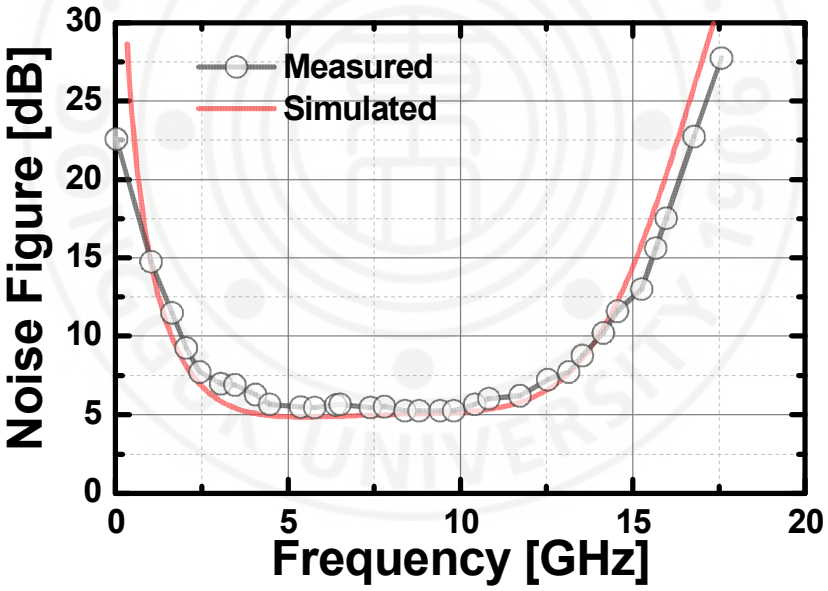


Figure II-6. Measured and simulated results of NF for the LNA.

On-chip measurements of the phase linearity (group delay variation) and S-parameters of the LNA were carried out by Keysight N5224A PNA. Figure II-4 shows the measured and simulated S-parameters. Within 1 – 13 GHz, the measured maximum value of S_{21} is 18.21 dB at 8.75 GHz, and the minimum value of it is 13.12

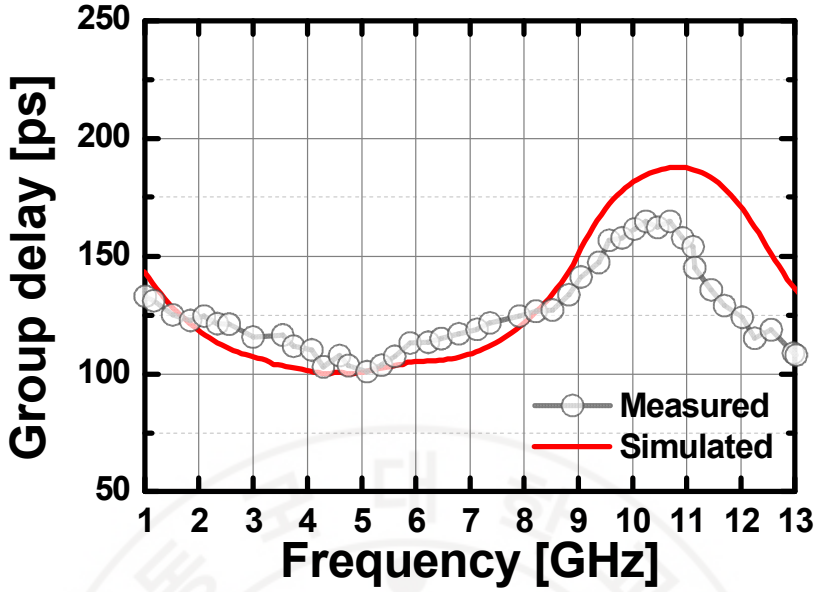


Figure II-7. Measured and simulated results of group delay for the LNA.

dB at 6 GHz. In this frequency range, the measured input and output return-loss are better than 10 dB, and the measured 3-dB bandwidth of the power gain is wider than 12 GHz. The measured results correspond well with the simulation, as illustrated in Figure II-4. As can be seen the Figure II-5, the input-referred 1 dB compression point (IP_{1dB}) was measured by gradually increasing the input power level at 11 GHz, and the result depicts -21.43 dBm of IP_{1dB}. The noise figure measurement was performed with Agilent N8975A noise figure analyzer. The measured and simulated noise figures of the LNA are shown in Figure II-6. The minimum NF is 5.28 dB at 9.4 GHz. The measured and simulated group delay of the implemented amplifier are presented in Figure II-7. In the range of 3 – 11 GHz, the measured group delay variation is 101 psec at 5.1 GHz (165 psec at 10.6 GHz) and the group delay variation is around ± 31 psec.

So as to assess the performance of the proposed LNA, the figure-of-merit (FOM) is given by [35]:

$$FOM\left[\frac{GHz}{mW}\right] = \frac{|S_{21}|[dB] \times BW[GHz]}{|NF-1|[dB] \times Power_{DC}[mW]} \quad (2\text{-}3)$$

Table II-1. Summary of the proposed LNA and comparison with previously published CMOS LNAs.

LNA	**This work**	**[32]**	**[33]**	**[34]**
Tech. [nm]	65	180	130	90
Freq. [GHz]	1 - 13	3.1 - 10.6	2 – 9.6	3.1 – 10.6
G_{MAX} *[dB]*	18.21	12.26	11	22.6
S_{11} *[dB]*	< -10	< -11.8	< -8.3	< -10.5
NF_{min} *[dB]*	5.28	4.24	3.6	5.5
IP_{1dB} *[dBm]*	-21.43	-22	-16.5	-19.7
Group delay variation [psec]	134±31	90.9±29.8	NA	73±41
P_{DC} *[mW]*	14.92	10.34	19	34.8
FOM	3.42	2.74	1.69	1.08

Table II-1 contrasts the performance summary for the implemented transformer-based UWB LNA with previously reported CMOS wideband LNAs. The proposed LNA accomplishes better FOM than references in [32-34].

III. Compact I/Q Up-Conversion Chain for a 5G Wireless Transmitter

3.1. Introduction

The emerging fifth-generation wireless standard (5G) in the millimeter-wave regime is aimed at achieving higher speed data transmission and higher capacity with high-quality communication. Recently, a prototype system for 5G mobile communications using the millimeter-wave band has been successfully demonstrated [36-37].

In CMOS wireless transceiver, the direct-conversion architecture is widely used for mobile communication since not only can it be miniaturized, it can also reduce power consumption compared to heterodyne architecture [38-39]. However, in implementing a highly integrated millimeter-wave transceiver with multiple channels, the superheterodyne architecture is more reliable [37]. Specifically, the intermediate frequency (IF) upconverter should be carefully designed with a suppressed in-phase/quadrature (I/Q) mismatch, and it has to provide high linearity. A variety of studies have reported the improvement of the linearity of a CMOS upconverter, such as voltage feedback with adaptive biasing schemes [40], and a resistive feedback network with inter-stage inductor [38], but these approaches consume a large amount of chip area. In [39], a complementary derivative superposition technique [41] was applied to achieve high linearity. However, the reported quadrature signal generator (QSG) occupies most of the chip area, which is inappropriate for a 5G wireless transceiver with integrated multifunctional blocks.

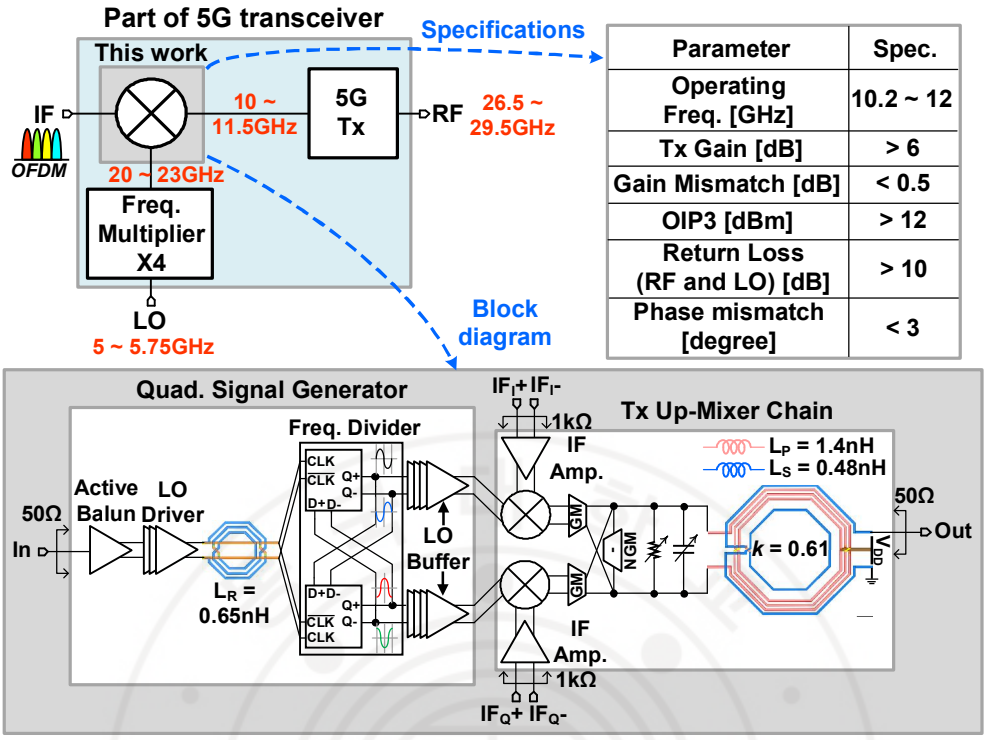
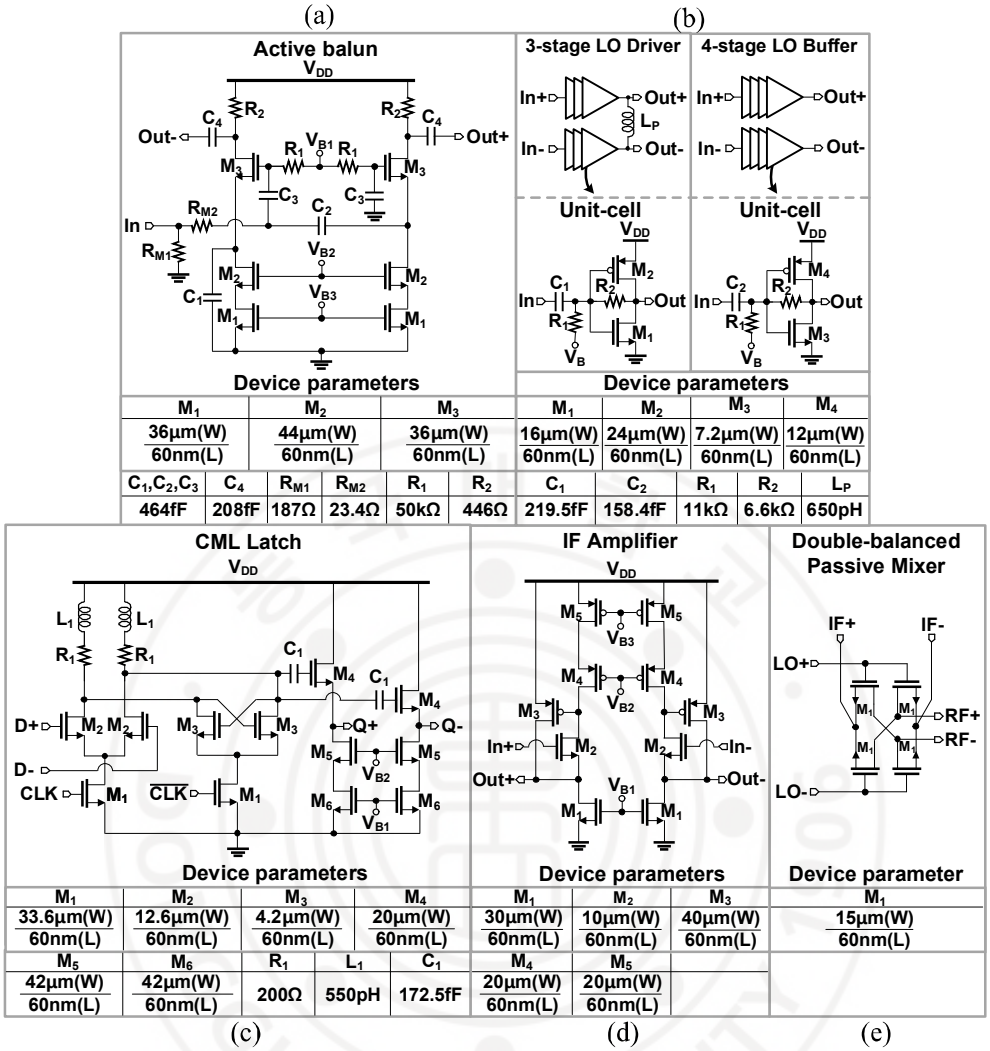


Figure III-1. A block diagram and the specifications of the proposed up-conversion mixer for a 5G wireless transmitter [37]. The mixer consists of a quadrature signal generator and a Tx up-conversion chain [42].

3.2. Design of the I/Q Upconverter

A block diagram of the designed I/Q upconverter with a QSG is presented in Figure III-1 [42]. The designed Tx up-conversion chain consists of an intermediate frequency (IF) amplifier, an I/Q double-balanced passive mixer for low flicker noise [45], a current-mode GM stage with a cascode amplifier, variable resistor and digital capacitor-bank for tuning the center frequency, and a transformer-based balun for single-ended output. A negative gm (NGM) cell implemented with a cross-coupled pair is connected in parallel with the output of the GM stage, which operates in a weak inversion to cancel the 2nd derivative of g_m which mainly contributes to IM3 in the GM stage [43-44]. A super-source follower which has local feedback through M3 (Figure III-2 (d)) is used to drive the low IF input resistance of the passive mixer, and it provides a high load impedance to the variable gain amplifier in voltage mode at the baseband. The double-balanced passive mixer shown in Figure III-2(e) is employed to perform an up-conversion with high linearity and low-flicker noise. The



Active balun						
M_1	M_2	M_3				
36μm(W)/60nm(L)	44μm(W)/60nm(L)	36μm(W)/60nm(L)				
C_1,C_2,C_3	C_4	R_{M1}	R_{M2}	R_1	R_2	
464fF	208fF	187Ω	23.4Ω	50kΩ	446Ω	

3-stage LO Driver / 4-stage LO Buffer				
M_1	M_2	M_3	M_4	
16μm(W)/60nm(L)	24μm(W)/60nm(L)	7.2μm(W)/60nm(L)	12μm(W)/60nm(L)	
C_1	C_2	R_1	R_2	L_P
219.5fF	158.4fF	11kΩ	6.6kΩ	650pH

CML Latch					
M_1	M_2	M_3	M_4		
33.6μm(W)/60nm(L)	12.6μm(W)/60nm(L)	4.2μm(W)/60nm(L)	20μm(W)/60nm(L)		
M_5	M_6	R_1	L_1	C_1	
42μm(W)/60nm(L)	42μm(W)/60nm(L)	200Ω	550pH	172.5fF	

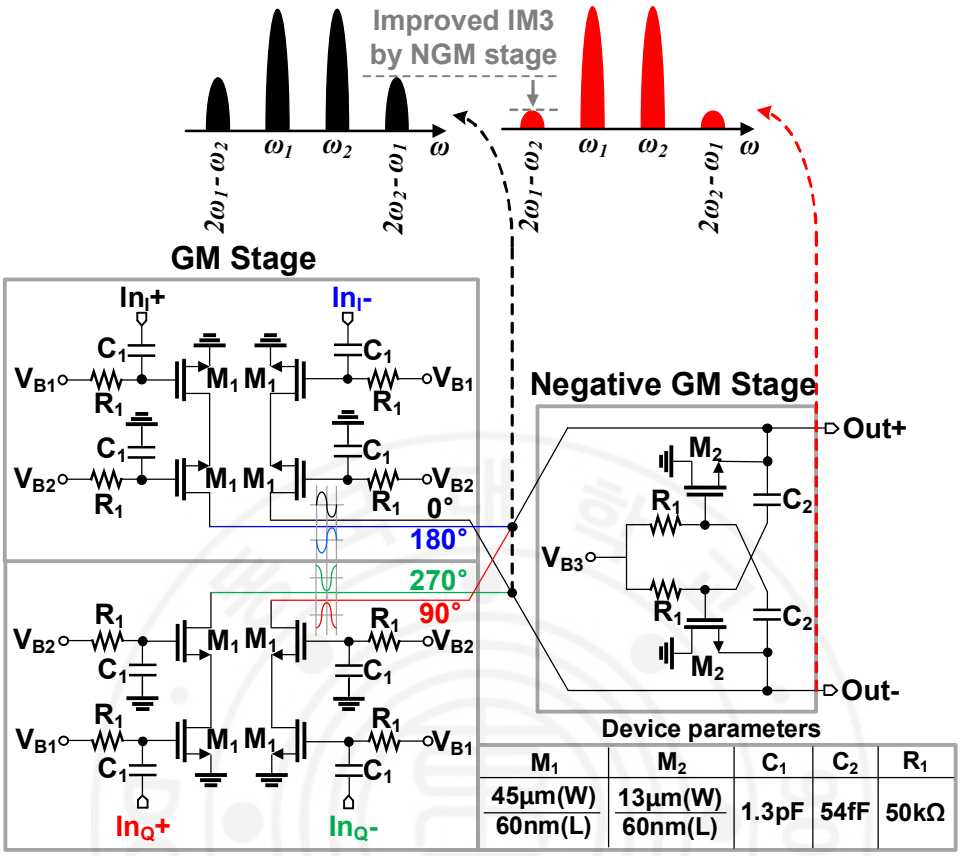
IF Amplifier				
M_1	M_2	M_3		
30μm(W)/60nm(L)	10μm(W)/60nm(L)	40μm(W)/60nm(L)		
M_4	M_5			
20μm(W)/60nm(L)	20μm(W)/60nm(L)			

Double-balanced Passive Mixer	
M_1	
15μm(W)/60nm(L)	

Figure III-2. Schematics of the (a) active balun, (b) unit-cells for the LO driver and buffer, (c) CML latch, (d) IF amplifier, and (e) double-balanced passive mixer.

double-balanced mixer can also improve both LO-to-IF and IM2 performance owing to its balanced structure. By utilizing rail-to-rail LO signals with 25% of the duty cycle from the QSG, a 3dB higher gain can be obtained with smaller nonlinearity and noise contribution from the mixer compared with when using 50% of the duty cycle [46]. The up-converted I and Q signals from each mixer are combined in current mode through the GM stage with cascode devices, as shown in Figure III-3.

The QSG with a 25% duty cycle consists of an active balun, a 3-stage CLK driver, a frequency divider implemented with two CML D-latches, and a 4-stage LO driver.



M_1	M_2	C_1	C_2	R_1
45μm(W) / 60nm(L)	13μm(W) / 60nm(L)	1.3pF	54fF	50kΩ

Figure III-3. Schematic of the GM and NGM stages. It is noteworthy that the IM3 of the up-converted signal can be improved through the NGM stage.

It converts the single-ended 2fLO signal to the 25% duty cycle I/Q (0°/90°/180°/270°) signals used for the LO driving signals of the passive mixer. To generate a differential output signal from a single-ended sinusoidal CLK signal of -10dBm, an active balun is implemented using common gate and common source stages in parallel, as shown in Figure III-2(a). Since the size of the active balun is only 65μm^2, it can consume less chip area than passive balun (> 180μm^2 at 20GHz). The rail-to-rail output voltage swing of the active balun is achieved by using the CLK driver consisting of three-stage self-biased inverters, as shown in Figure III-2(b). A shunt inductor of 650pH is placed to compensate for part of the loading capacitance for driving the loading capacitance from the CML D-latches. Since an I/Q mismatch of the LO signal generated by the QSG directly affects the error vector magnitude performance of the transmitter, the required gain and phase mismatch in the upconverter should be less than 0.5dB and 3°, respectively [47]. It can be seen that

the QSG with the frequency divider with two high-speed D-latches with inductive peaking combined with the cascaded self-biased inverters is a quite appealing approach to meet the gain and phase error requirements while occupying a relatively compact area. Finally, the output I and Q signals generated by the frequency divider are amplified to provide rail-to-rail swing to the LO of the double-balanced mixer using the LO buffer, as presented in Figure III-2(b).

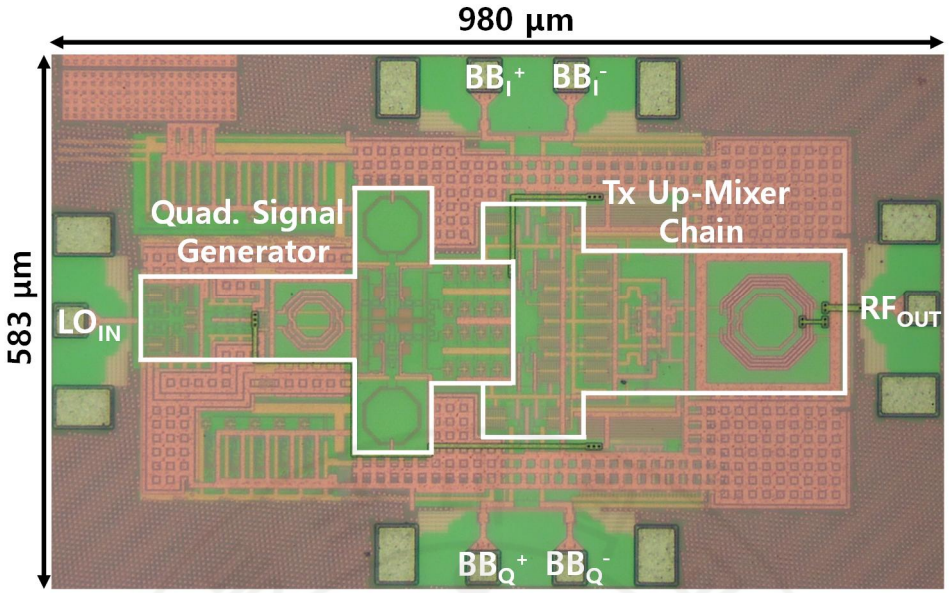


Figure III-4. A photograph of the chip with the proposed up-conversion mixer with the QSG (chip size: 0.58 x 0.98mm^2).

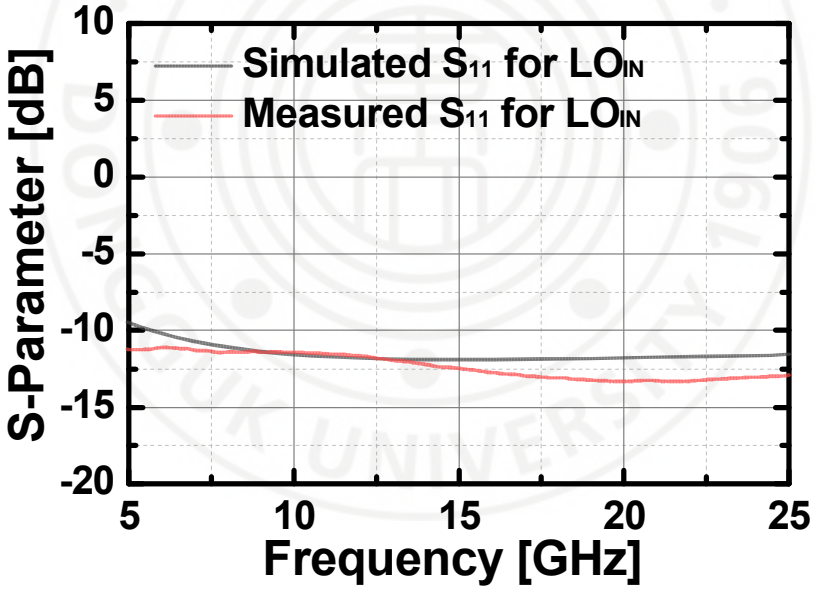


Figure III-5. Measured and simulated S_{11} for LO_{IN}.

3.3. Measurement results

The proposed Tx upconverter was implemented with a 65-nm CMOS process. Figure III-4 presents a microphotograph of the chip of the I and Q upconverter block (the chip occupies 0.58 × 0.98mm^2). The implemented up-conversion chain

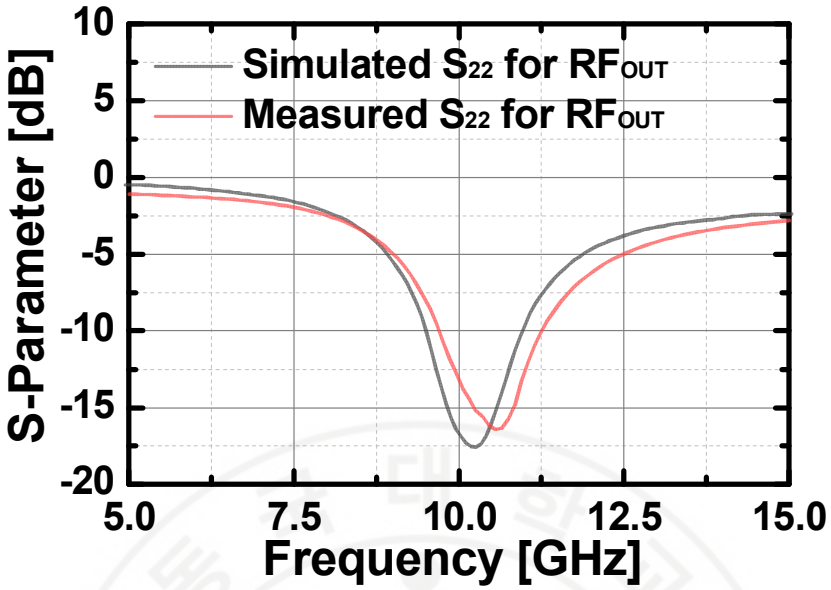


Figure III-6. Measured and simulated S_{22} for RF_{OUT}.

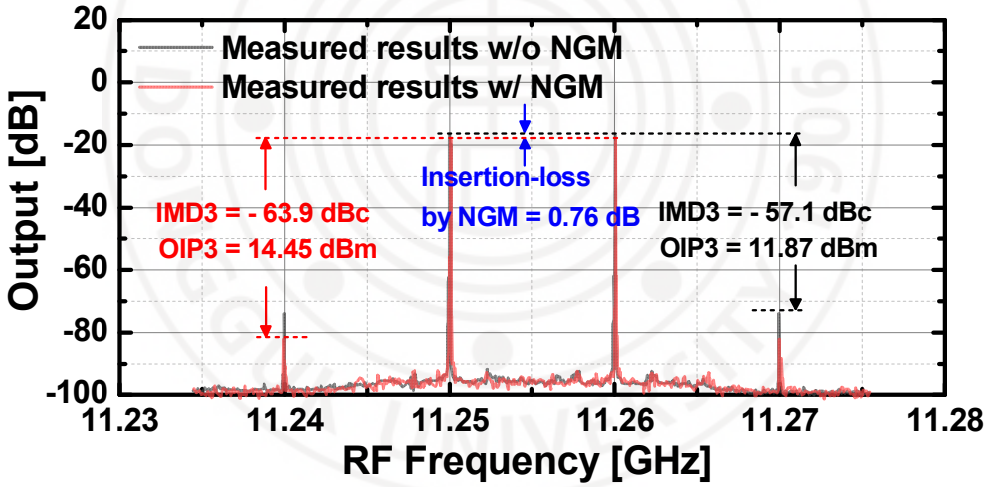


Figure III-7. Measured up-converted RF output results with and without the NGM stage.

consumed 48.7mW (QSG: 24.3mW, Up-mixer chain: 24.4mW) from a 1V supply, and digitally controlled through a serial-peripheral-interface (SPI) scan-chain.

On-chip measurements of the S-parameters were performed with E8361C PNA network analyzer, the conversion gain and output third-order intercept point (OIP3) measurements were performed with a Keysight N9030A PXA spectrum analyzer, a

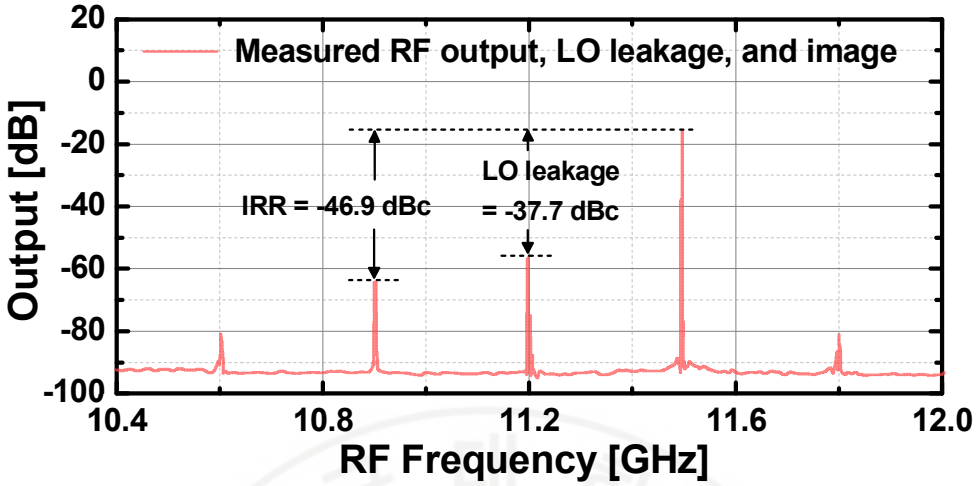


Figure III-8. Measured RF output, LO leakage, and image with a single-tone input signal.

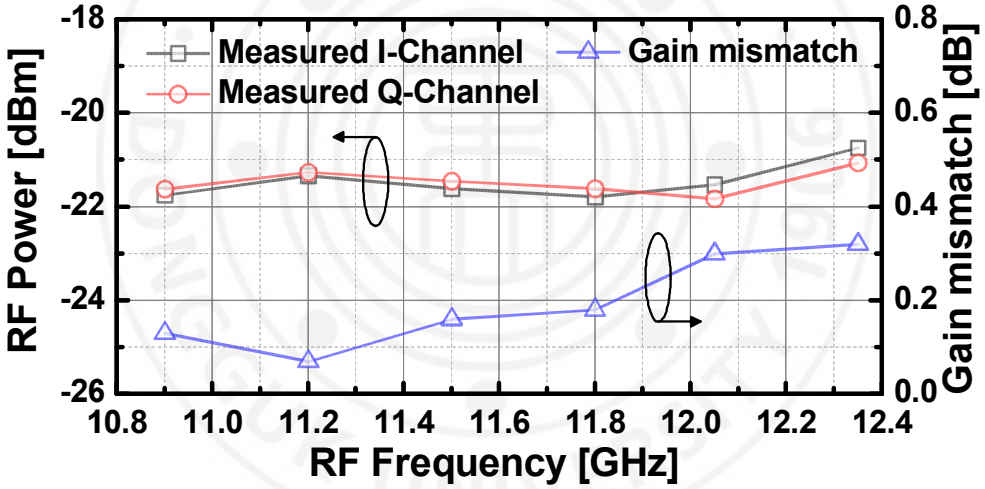


Figure III-9. Measured up-converted RF output results for the I/Q channels with less than 0.2dB of gain mismatch.

Keysight E8257D analog signal generator for the LO signal, and a Rohde & Schwarz SMW200A vector signal generator for the differential I/Q baseband signals. Figures III-5 and III-6 show the measured S-parameters which corresponded well with the simulation. Figure III-7 presents a comparison of the measured output spectrum with two-tone IF inputs of 100Mz and 110MHz with and without activating the NGM cell, the measured OIP3 with NGM was 14.45dBm while the OIP3 without NGM was

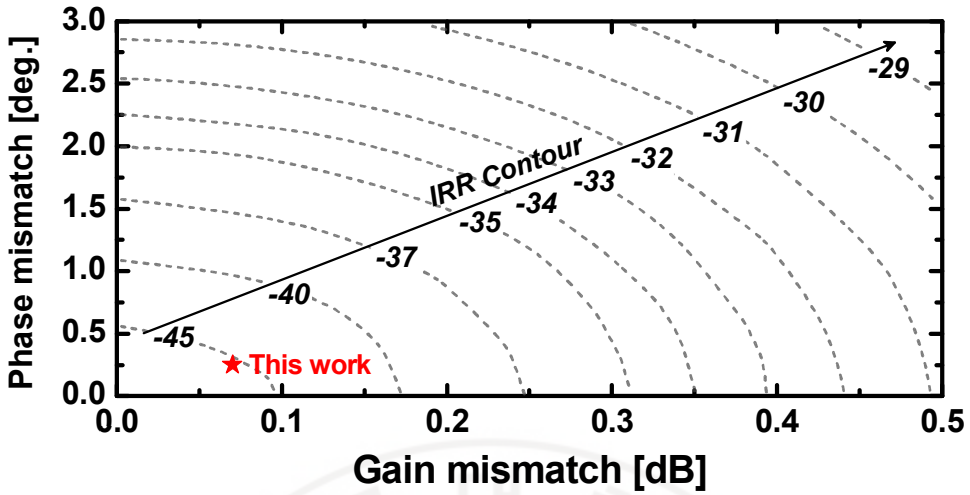


Figure III-10. Phase mismatch based on the measured gain mismatch and IRR contour. The phase mismatch was expected to be lower than 0.5degrees.

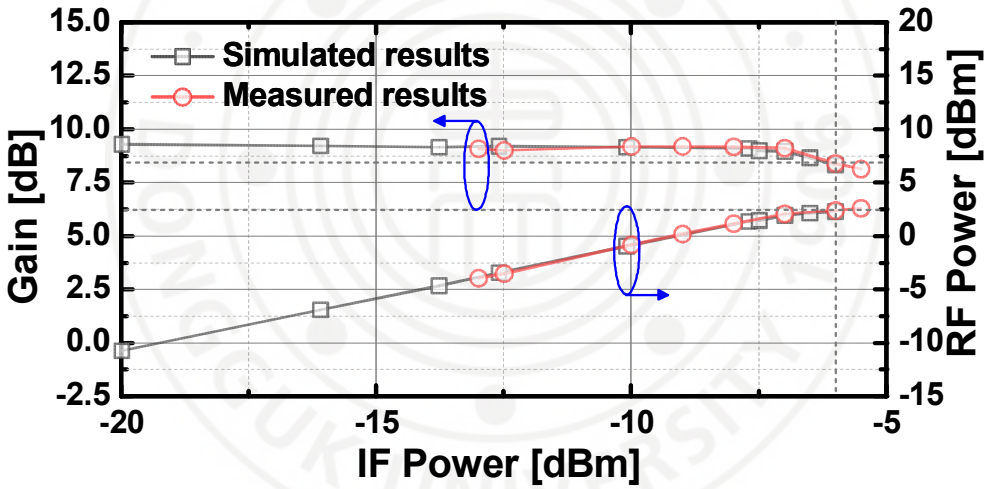


Figure III-11. Measured and simulated results of gain and RF power for the implemented upconverter depending on IF power with f_{IF} = 300Mz and f_{LO} = 22.4GHz.

only 11.87dBm, which shows +2.58dB of improvement owing to the 3rd harmonic cancellation with a negligible extra power consumption of 438μW. On the other hand, when the NGM is turned on, the insertion-loss is lower than 1dB. For the measurement of the image rejection ratio (IRR), a single-tone IF input with a frequency of 300MHz was applied at the IF input port of the mixer. As shown in Figure III-8, the measured LO leakage and IRR were -37.7dBc and -46.9dBc,

Table III-1. Comparison with previously reported up-conversion mixers.

Reference	**This work**	**[38]**	**[39]**	**[40]**
Technology	65nm	65nm	65nm	0.13μm
LO Freq. [GHz]	20 ~ 23	51 ~ 69	28	18.9 ~ 29
RF Freq. [GHz]	10 ~ 11.5	60	27.6 ~28.4	23.4 ~ 29.2
P_{LO} *[dBm]*	-10	0	-13	0
Gain	9.12	6.2	11.4	-1.9
OP_{1dB} *[dBm]*	2.65	-7.3	2	0.3
OIP3 [dBm]	14.45	N/A	15.7	N/A
Chip area [mm2]	0.57**	0.42*	1.23**	0.86***
P_{DC} *[mW]*	48.7**	17.8*	15*	39.3***

* Mixer only, ** Mixer with quadrature signal generator, *** Mixer with LO buffer

respectively. Figure III-9 shows the measured gain mismatch of I/Q channels by varying LO frequency for a fixed IF frequency (P_{IF}=-30dBm at f_{IF} = 300MHz), which was lower than 0.2dB. Based on the measured gain mismatch and IRR, we expect that the phase mismatch for the mixer was lower than 0.5degrees (Figure III-10). The measured gain and output power depending on IF input power closely matched the simulation results, as presented in Figure III-11. Table III-1 compares the implemented mixer with previously reported up-conversion mixers [38-40]. The designed mixer with quadrature signal generator in the upconverter showed the smallest chip size.

IV. 2–18 GHz Compressed Sensing Receiver with Broadband LO Chain

4.1. Introduction

Good control and analysis of the spectrum are important in applications for protection and defense. The traditional method, based on the Nyquist sampling principle, allows an ultra-fast analog-to-digital converter (ADC) with a sampling frequency greater than twice the average frequency of the transmitted signal to track an unseen signal in real time. While more than 10 Gb/s, or even better, interleaved ADCs have recently been proposed as Integrated Circuits (ICs) [14], the ultra-fast back-end module for microwave signal monitoring still needs tens of watts of power, and its size is considerably voluminous. It is therefore very challenging to implement a microwave sensing receiver which collects and processes unidentified signals with the Nyquist sampling rate in real time. The airborne surveillance systems in particular need miniaturized microwave monitoring receivers with low power consumption [15], [48].

Recently, a compressed sensing receiver capable of real-time signal restoration was introduced as an excellent solution to avoid the above-mentioned problems by obtaining a very high compression ratio between the Nyquist rate and the ADC sampling rate at the back-end. In [48]–[51], researches for the compressed sensing architecture have been carried out. It can be possible the reconstruction of the signal even with a sub-Nyquist sampling frequency using a random sensing matrix that satisfies the requirement of the restricted isometry property (RIP) [53] when the input signal is sparse. The pseudo-random bit sequence (PRBS) signal [52-53], is the most commonly employed sensing array.

Based on the proven compressed sensing theory several compressed sensing receivers (CSRXs) were published in the literature [48-50] to track broadband RF signals in real time. However, the realization of a microwave CSRX with the broadband PRBS generation and the high-swing local-oscillator (LO) signal transmission to the down-converting mixer without severe spectrum distortion of the PRBS signal is challenging.

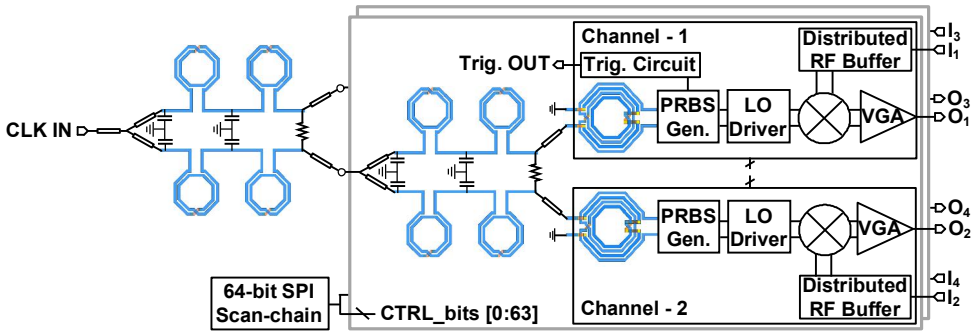


Figure IV-1. A block diagram of the integrated 4-channel compressed sensing receiver in a 0.13-μm BiCMOS [54].

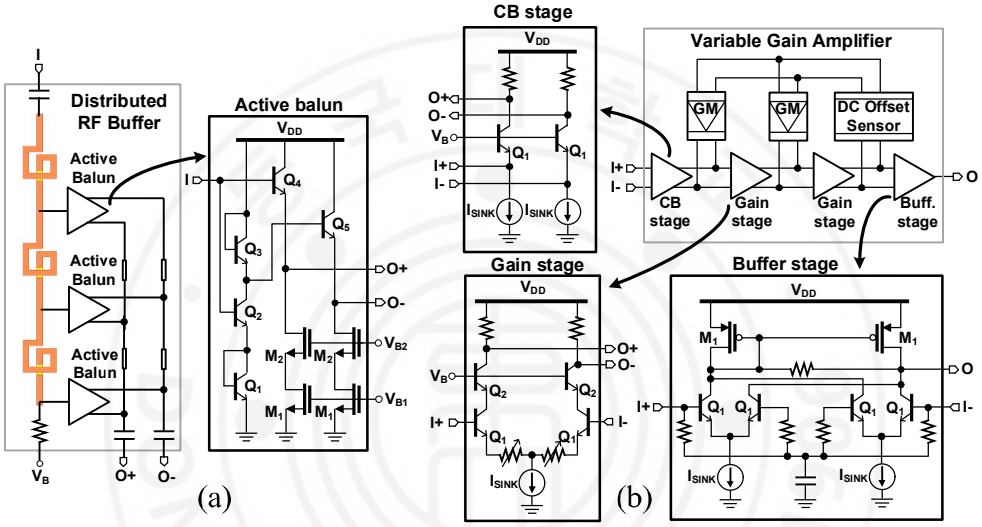


Figure IV-2. Schematics of (a) the distributed RF buffer and (b) the variable gain amplifier [54].

4.2. The compressed sensing receiver design

In order to support the improved compression ratio, four independent receiving channels with a 36-Gb/s PRBS generator having a band-equalized LO chain are integrated to the CSRX, as shown in Figure IV-1 [54].

A 2–18 GHz distributed amplifier configured with three active balun cells, a four-stage variable gain amplifier (VGA), and a double-balanced passive mixer are included in the broadband receiver. The passive mixer is driven by the active balun, which transforms the single-ended input to the balanced output in the current mode. As shown in Figure IV-2(a), in order to the characteristic impedance Z_0 = 50 Ω over 2–18 GHz at the RF input, a distributed LC network is constructed as the pseudo-transmission line.

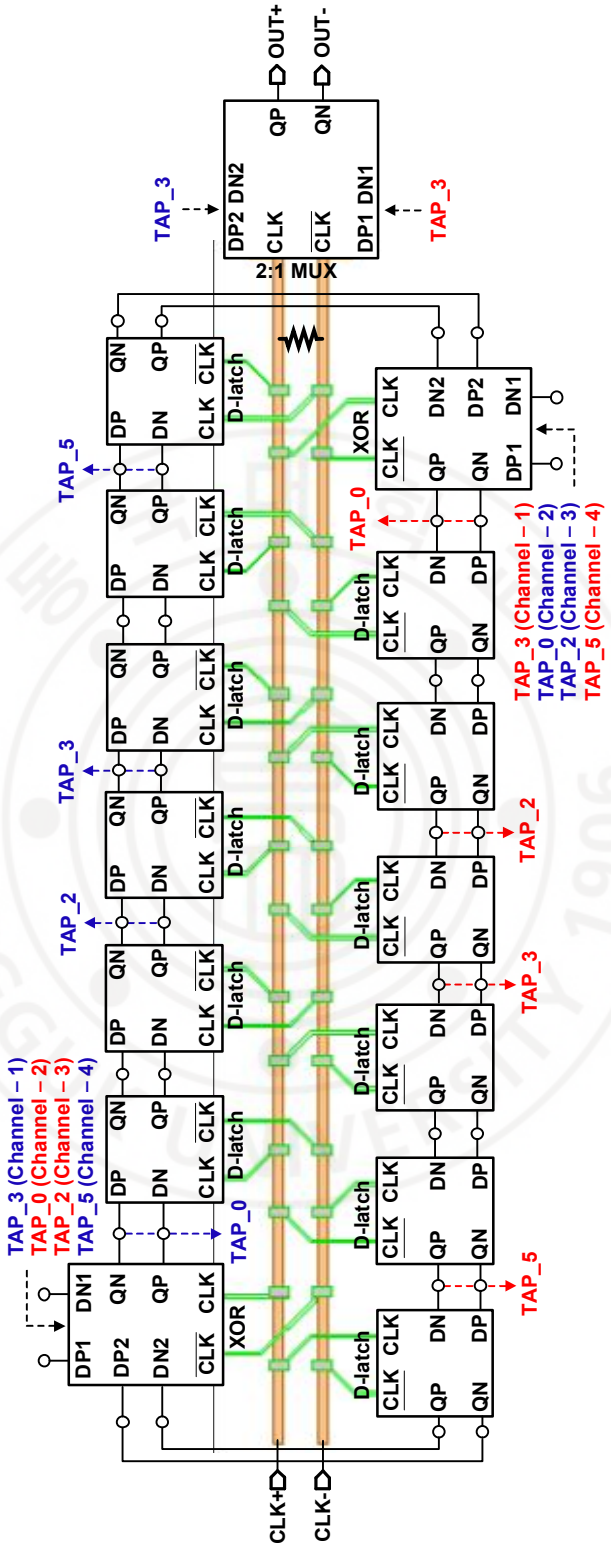


Figure IV-3. Block diagram of PRBS generator.

The intermediate frequency (IF) signal in the range of 100 kHz to 500 MHz is amplified by the VGA from the IF port of the mixer. For the low input impedance and the improved linearity, the first stage for the VGA is the common base, which makes the mixed IF current to easily deliver to the VGA, as shown in Figure IV-2(b). The cascode amplifiers are used in the 2nd and 3rd gain stages. To change the variable gain, the source degenerated resistors and the variable 4-bit resistor-bank are implemented in each of these. So as to drive the external back-end block through the 50-Ω CPW on the PCB, the output buffer is realized.

Since the PRBS LO signal is composed of multiple sets of tones which extend even into the IF band, the LO-to-IF isolation is most critical issues in the CSRX design. Thus, the double-balanced mixer is built to obtain high isolation between the mixer`s LO and IF ports by canceling out the balanced LO leakages at the mixer`s IF port where the lowest LO tone is 280 MHz.

As the sensing matrix of each CSRX channel, a 36-Gb/s PRBS generator with half-rate 36-Gb/s PRBS signal, which is integrated as the LO mixing signal, was introduced. In order to implement the 36-Gb/s PRBS generator, an interleaved linear-feedback shift register (LFSR), two XORs, and a 2:1 multiplexer (MUX) by using the "cycle-and-add" nature of the m-sequence signal [56] are integrated, as shown in Figure IV-3. The 36–Gb/s 2^7-1 PRBS can be generated by seven consecutive flip-flops with a half-rate clock (CLK) frequency of 18 GHz coming from the CLK distribution network. According to the characteristic polynomial x7+x6+1, the designed architecture generates L = 127 of the sequential length. In the Fibonacci LFSR, an XOR play a role in the feedback circuit. Taps (3,6), (0, 6), (2, 6), and (5, 6) are used as the input for the channel-1, channel-2, channel-3, and channel-4 PRBS patterns, respectively. So as to provide f_{clk} = 18 GHz to each channel evenly, three lumped-element Wilkinson dividers are integrated in the CSRX. All the variables are digitally controlled by using a 64-bit serial-peripheral-interface (SPI) scan-chain.

The spectrum of the PRBS (m-sequence) signal is made up of an abundant amount of harmonic tones of $f_p = f_{PRBS}/L$ = 280 MHz resulting in a broadband sinc-shaped spectrum. Thus, the 36-Gb/s PRBS generator`s the high-frequency spectrum

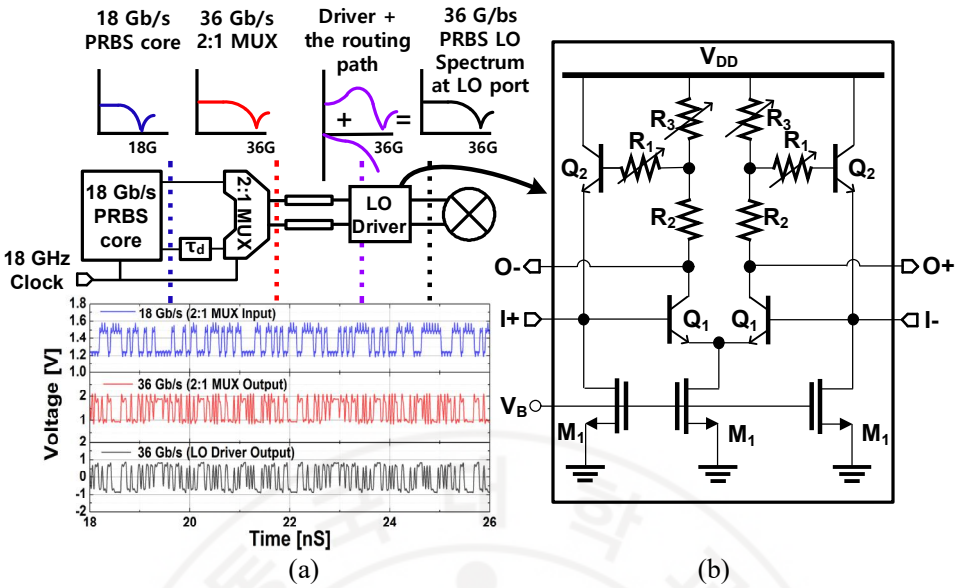


Figure IV-4. (a) A block diagram and the frequency response of the band-equalized LO generator and simulated PRBS pattern and (b) a schematic of the LO driver.

with the 2:1 MUX is specifically influenced by the the LO driving chain having a low-pass response and frequency response of the MUX due to parasitic capacitances. As a results, it can be difficult to achieve successfully compressed sensing caused by the severely distorted high-frequency harmonic tones from the PRBS generator. In order to solve this problem, a feedback amplifier is designed to provide a broadband input matching and the gain peaking at the designated high-frequency region as well as to equalize the high-frequency response of the LO signal after the 2:1 MUX of the PRBS generator, as shown in Figure IV-4(b). A shunt-shunt feedback network is constructed with Q_2, R_1, R_2, and R_3. The peaking of the frequency response can be controlled by the ratio of R_1/R_2 and R_3/R_2 [57]. Figure IV-4(a) shows the simulated PRBS pattern at the LO port of the mixer as well as at the input and output of the 2:1 MUX.

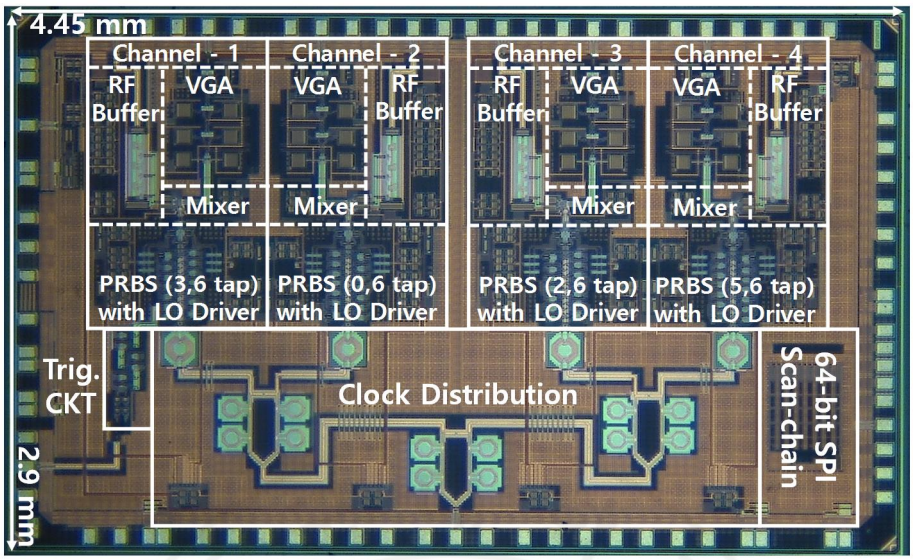


Figure IV-5. A microphotograph of the implemented 4-channel CSRX chip (chip size = 2.9 × 4.45 mm^2)

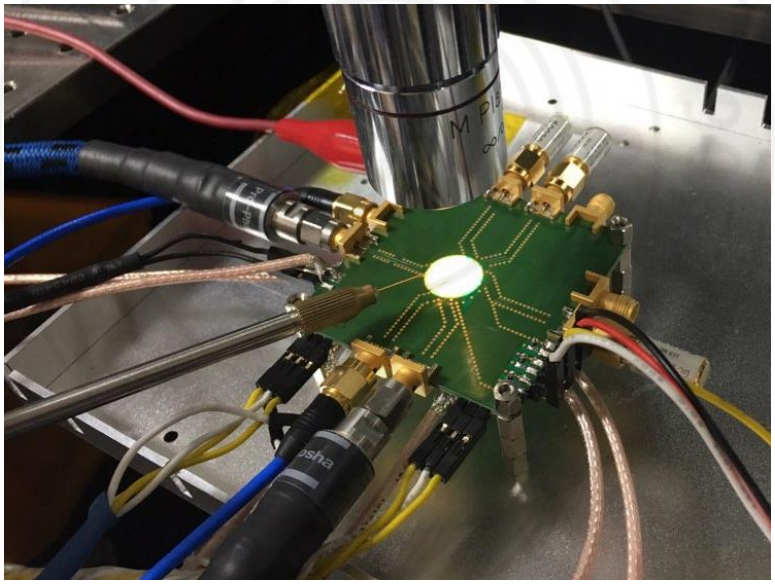


Figure IV-6. The PCB of the packaged CSRX chip for the measurement.

4.3. Measurement results

With f_T = 230 GHz, the CSRX was realized in STMicroelectronics 0.13-μm BiCMOS process. A chip photograph of the implemented four-channel CSRX is shown in Figure IV-5. The area of the fabricated chip is 2.9 × 4.45 mm^2. The packaged CSRX chip on the PCB is depicted in Figure IV-6. The measured results

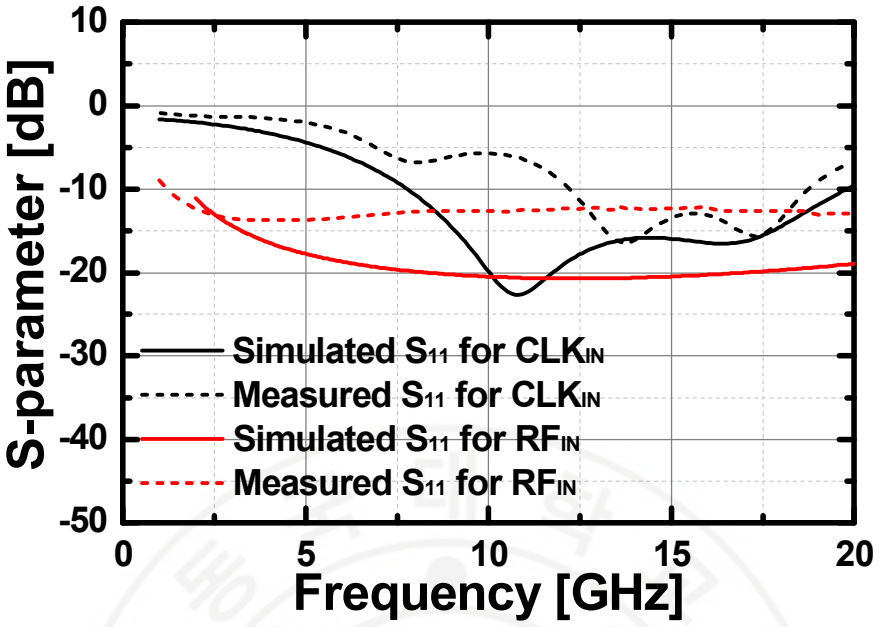


Figure IV-7. Measured and simulated S_{11} results for the CLK and RF inputs in the CSRX.

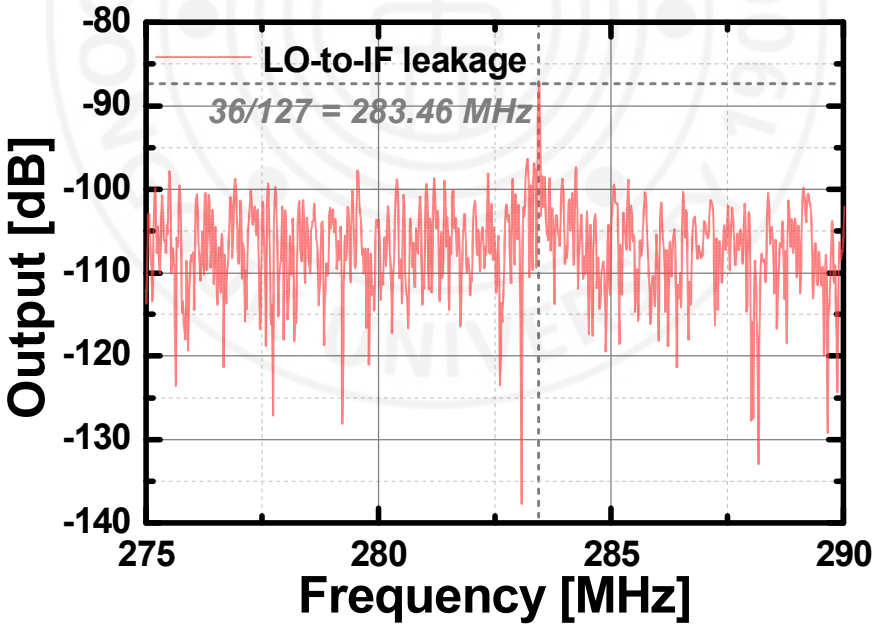


Figure IV-8. Measured LO-to-IF leakage at 18 GHz CLK input.

for S_{11} of the LO CLK and RF input are shown in Figure IV-7. The return loss of the CLK input port was around 15 dB at f_{clk}=18GHz, and that of the RF input port was

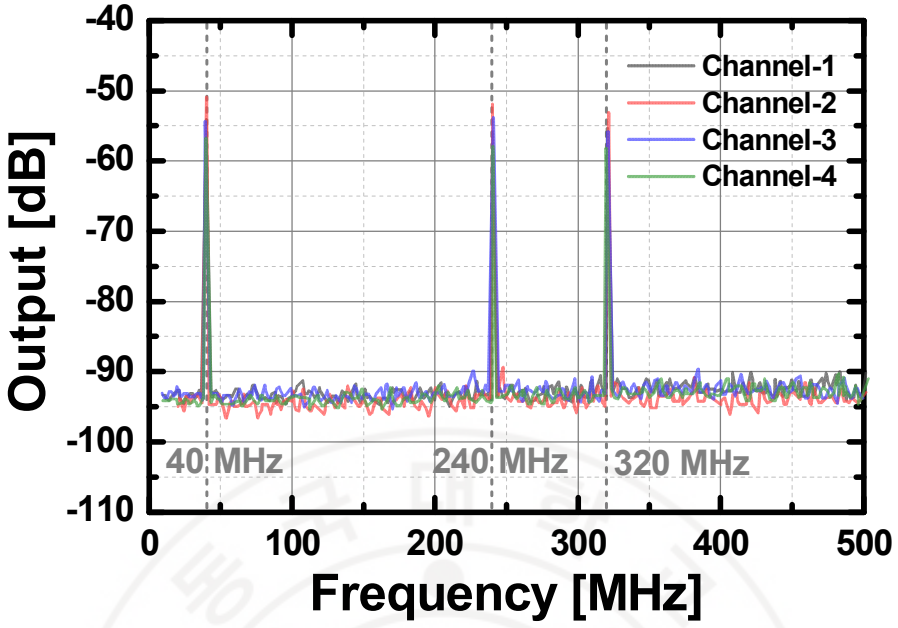


Figure IV-9. Measured IF output at 40 MHz, 240 MHz, and 320 MHz with a single tone input at f_{RF} =2 GHz for four independent CSRX channels.

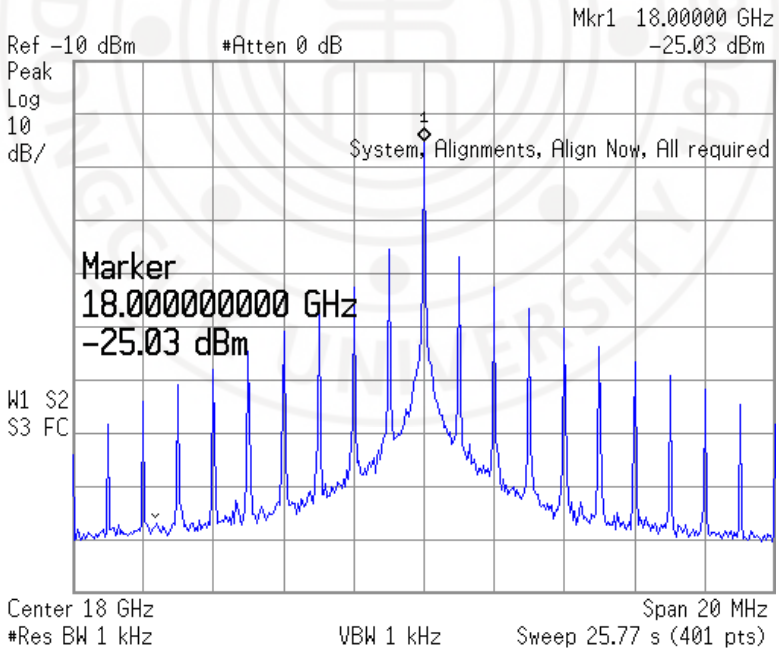


Figure IV-10. Spectra of the 18 GHz RF input signal (FM with a pulse signal).

better than 10 dB over the aimed 2-18 GHz range. As shown in Figure IV-8, the measured LO-to-IF leakage was around 90 dB.

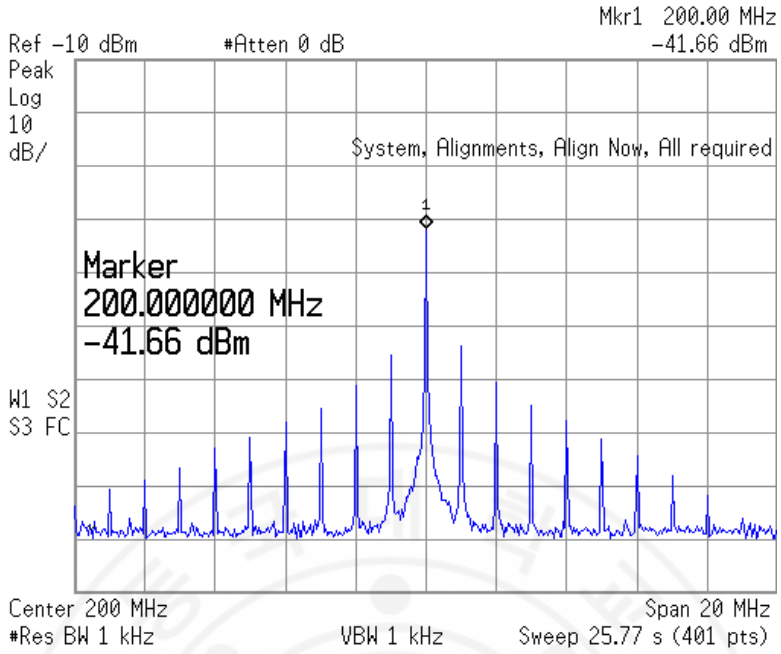


Figure IV-11. One of the sensed repetitive IF signal of the FM input at 18 GHz with a pulse signal in the CSRX.

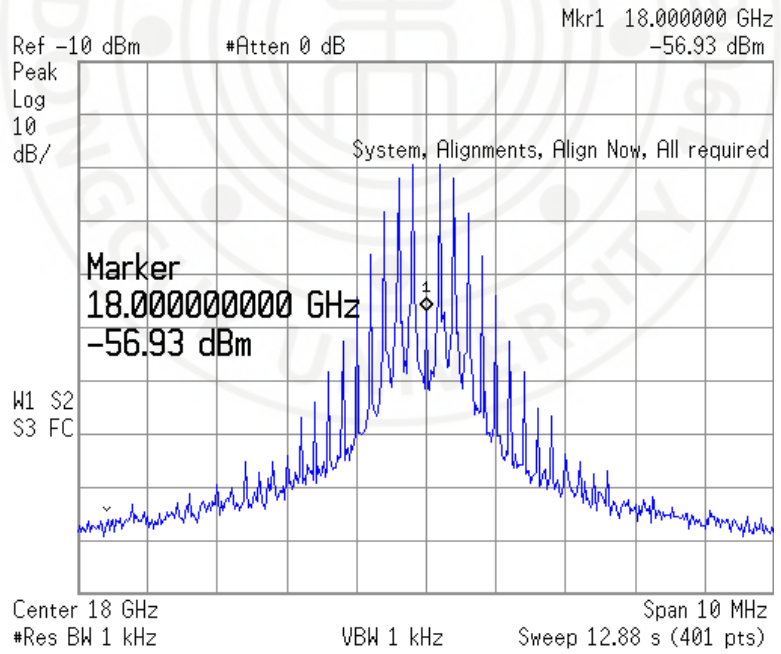


Figure IV-12. . Spectra of the 18 GHz RF input signal (FM with a ramp signal).

A sinusoidal input signal with f_{RF} = 2 GHz using an Agilent 83623B signal generator is firstly applied to verify the microwave compressed sensing. In order to

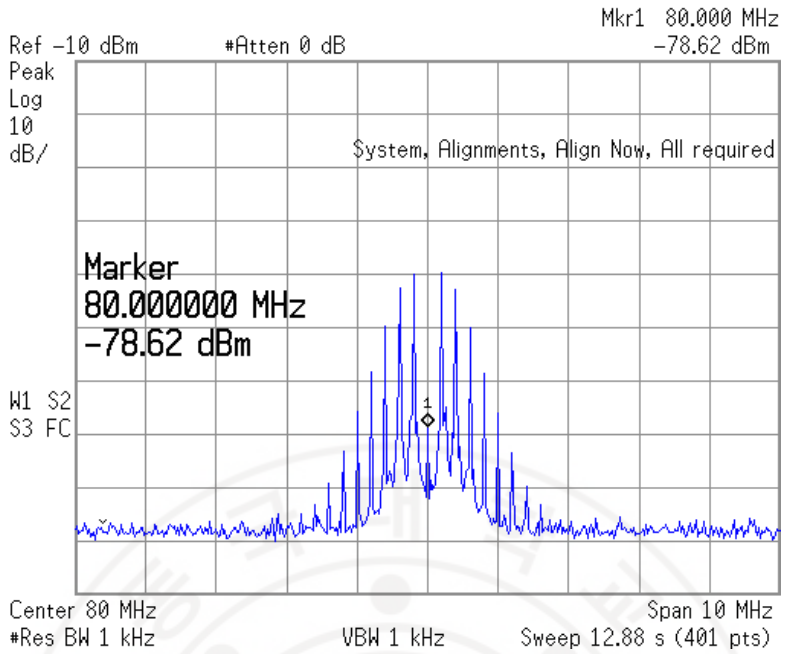


Figure IV-13. One of the sensed repetitive IF signal of the FM input at 18 GHz with a ramp signal in the CSRX.

Table IV-1. Comparison with previously reported state-of-art CSRXs in integrated spectrum sensors.

Ref.	**This work**	**[48]**	**[49]**	**[50]**
Process	ST 130 nm BiCMOS	NG 450 nm InP	ST 65 nm CMOS	IBM 90 nm CMOS
f_T/f_{max}	230 GHz 280 GHz	> 300 GHz > 300 GHz	> 300 GHz > 300 GHz	155 GHz 60 GHz
Die Area	12.9 mm2	17.6 mm2	1.96 mm2	8.85 mm2
S_{11}	< - 10 dB	N/A	< -10 dB	< -15 dB
Input Range	2~18 GHz	0.1~2.5 GHz	2.7~3.7 GHz	0.1~2 GHz
Nyquist Rate	36 GHz	5 GHz	2 GHz	4 GHz
Compression Ratio	128.5	13.1	6.3	12.5
Channels	4	4	8 x I/Q	8
DC Power	1.95 W	6.1 W (w/ ext. ADC)	81 mW	506.4 mW

generate a 35.56-Gb/s PRBS pattern with f_p = 280 MHz, the half-rate clock signal of 17.78 GHz is applied at LO input port. With the f_{RF} = 2 GHz of the input tone, the measured repetitive IF output tones are well matched with the theoretical values (*i.e.*, 320 MHz = |2 GHz - 6×280 MHz|, 40 MHz = |2 GHz - 7×280 MHz|, and 240 MHz

= |2 GHz - 8×280 MHz|), as shown in Figure IV-9. Secondly, the frequency-modulated (FM) RF input from the Agilent 83623B signal generator with the center frequency f_{RF} of 18 GHz by modulating the pulse signal (Figure IV-10) is applied to the implemented CSRX chip. Lastly, the FM RF input from the Agilent 83623B signal generator with the center frequency f_{RF} of 18 GHz by modulating the ramp signal (Figure IV-12) is applied to the implemented CSRX chip. The reconstructed spectrum of the sensed IF signal corresponds well with that of the RF input signals, as shown in Figures IV-11 and IV-13. Table IV-1 compares the implemented CSRX with recently published state-of-the-art ones in integrated spectrum sensors [48-50]. As can be seen the comparison table, the designed CSRX shows the highest compression ratio.

V. Full X-band phased-array transmit/receive module chip

5.1. Introduction

Active phased-array antenna (APAA) systems have been extensively spotlighted in areas such as satellite communications, wireless communications, and radar applications owing to their increased channel capacity, reduced transmit power requirement, improved signal-to-noise ratio, and immunity to strong interference.

Until recently, phased array systems have been used primarily in defense and space applications since an electrically scanned APAA can support much faster beam scanning in a more compact volume than a mechanically scanned antenna. The traditional phased-array antenna system in defense and space applications has employed an expensive transmit/receive module (TRM) assembled with high-cost and bulky III-V MMICs [58-59] combined with a silicon-based baseband and digital control chip to achieve high performance.

Since hundreds or even thousands of TRMs can be incorporated in a phased array antenna system, depending on the application, it is essential that the TRM be compact, be low-cost, and have a low-power design without compromising its performance. Therefore, enormous amounts of research have been directed at silicon-based (SiGe BiCMOS or CMOS) fully integrated transceiver for the TRM in X-band APAA systems to resolve this challenging issue [60-73]. A successful design solution in conventional digital CMOS technology must address power consumption and production cost.

An all-RF phase shifting architecture (phase-shifting performed at RF frequencies) is usually used to construct typical APAA systems. Compared to an architecture that uses local oscillator (LO) or IF phase-shifting methods, an all-RF phased array architecture has excellent suppression of interference [62] with better linearity at the system level. It is a simple system with relatively low power consumption as it requires only a single high-performance receiver in the sum port, as illustrated in Figure V-1.

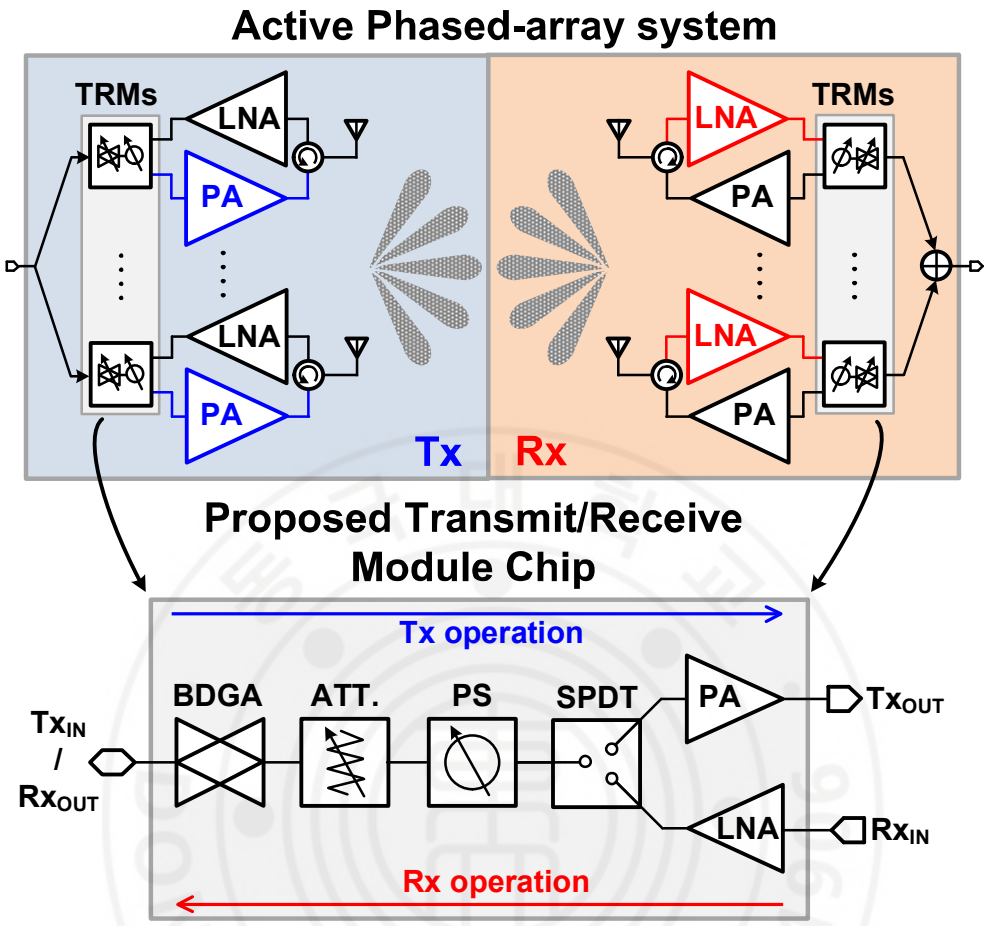


Figure V-1. Block diagrams of the active phased-array system and proposed transceiver configuration.

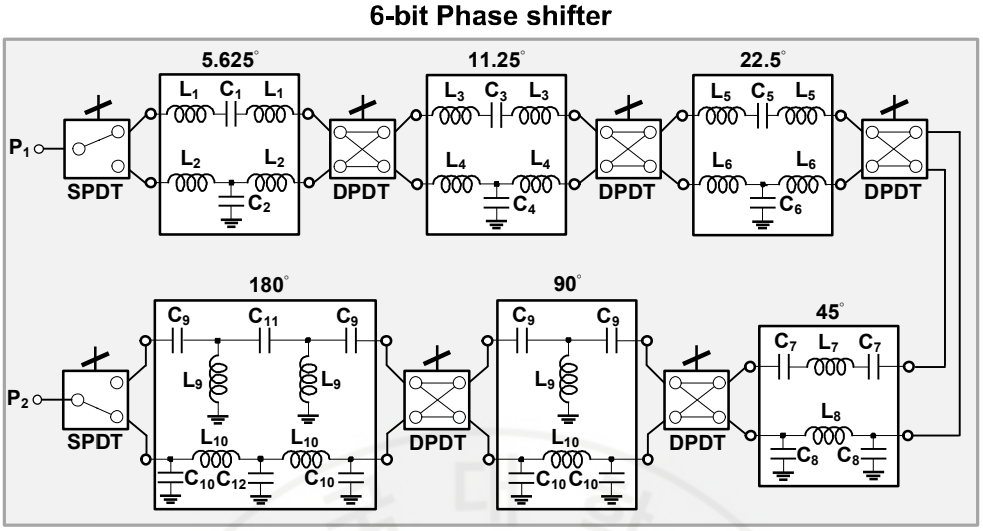
The RF phase shifter is a crucial element in phase array systems [74]. Therefore, in designing a TRM, its phase-shifting capability should be agile enough to steer the main lobe of the array antenna precisely, and its bandwidth should be wide enough to support various applications. In the design of wide-band phase shifters with high linearity and low power consumption in CMOS, the use of phase shifter topology configured with a high-pass (HP) / low-pass (LP) passive network has been widespread because it has negligible power dissipation, a simple control mechanism, and less reliance on the RF performance of the active device [75-76]. However, the HP/LP phase shifter only satisfies the desired phase shift with an acceptable port impedance match over a narrow frequency range. Thus, the inherent broadband characteristics of this type of phase shifter have not been efficiently deployed. Also,

the conventional iterative design approach takes more time to achieve the required bandwidth and phase error.

In order to improve the operating frequency range of the passive phase shifter, we misaligned the resonant frequency of the HP/LP network from the center frequency using derived formulae. With this approach, more than 50 % of the operating range under 5° of RMS phase error was enhanced. A detailed analysis with derived design equations is presented in Section II.

A block diagram of the proposed X-band TRM chip is illustrated in Figure V-1. In comparison with [64-65], the proposed TRM chip utilizes not only a single SPDT (three SPDT switches in [64]), but also shared phase shifter and attenuator (separate phase shifters and attenuators for Tx and Rx path [65]) by employing a bi-directional gain amplifier (BDGA) in Tx and Rx operations. Therefore, the proposed architecture has the advantage of reducing path loss and chip occupancy. Moreover, a wideband operation of the passive phase shifter could be achieved by assigning two separate resonant frequencies for the leading/lagging networks for the phase-shifting units where we controlled the slopes of their phase responses to meet the desired phase shifts at the center frequency.

Since the output power and the noise figure of the bi-directional transceiver with two-ports [70, 72] was limited by the performance of the BDGA, we implement a TRM chip with an SPDT switch to add PA and LNA separately. Also, the SPDT switch was used as a duplexer to select the Rx/Tx signal for bi-directional operation. The Rx path of the SPDT switch is connected to the output of the LNA from the Rx input, while the Tx path is connected to the PA for improved Tx output power. The TRM chip was fabricated in 65-nm CMOS technology with eight copper metal layers and one aluminum metal layer, and the top layer (3 μm) was used for passive component design.



Device parameters

L_1	L_2	C_1	C_2	L_3	L_4	C_3	C_4	L_5	L_6	C_5	C_6
170 pH	100 pH	3 pF	80 fF	160 pH	120 pH	1.6 pF	95 fF	210 pH	180 pH	750 fF	135 fF

L_7	L_8	C_7	C_8	L_9	L_{10}	C_9	C_{10}	C_{11}	C_{12}
650 pH	515 pH	800 fF	145 fF	1.25 nH	510 pH	700 fF	145 fF	350 fF	290 fF

Figure V-2. Schematic and all device parameters of the proposed X-band 6-bit passive phase shifter using HP/BP/LP networks.

5.2. X-band transceiver design

5.2.1. 6-bit broadband passive phase shifter

The analysis presented in this section was contributed by Mr. Van-Viet Nguyen [77]. The implementation of the phase shifter was co-worked with Mr. Nguyen [77-78]. The typical structure of an HP/band-pass(BP)/LP phase-shifting cell includes third-order T-type HP filters, L-C-L BP filters, C-L-C BP filters and π-type LP filters as shown in Figure V-2 to minimize the number of inductors required. In comparison with [70, 72], we designed a 5.625° phase shift cell with BP and LP networks instead of switch to significantly enhance the operating frequency range. Inductors usually consume most of the chip area. The element values of each HP and LP network can be determined from its resonant frequency and the insertion phase at a given frequency by assuming that the network is well matched at its input and output ports (i.e., $|\angle S21|=\phi$ and S11=S22=0). The element values of the networks can be calculated as follows [79]:

$$L_1 = \frac{Z_0}{2\pi f_1 \sin(\phi_1)} \quad (5\text{-}1); \qquad C_1 = \frac{1}{2\pi f_1 Z_0 \tan(\phi_1/2)} \quad (5\text{-}2);$$

$$L_2 = -\frac{Z_0 \sin(\phi_2/2)}{2\pi f_2} \quad (5\text{-}3); \quad C_2 = -\frac{\tan(\phi_2/2)}{2\pi f_2 Z_0}, \quad (5\text{-}4)$$

where ϕ_1 and ϕ_2 are insertion phases of HP and LP networks at their resonant frequencies f_1 and f_2, respectively. In conventional design methodology, HP and LP networks are considered to resonate at the same frequency, that is, the center frequency of operation f_0. It is also assumed that each network has half of the expected insertion phase shift but with opposite signs at f_0. Each circuit element is calculated from (5-1) to (5-4) by setting $f_1 = f_2 = f_0$ and $\phi_1 = -\phi_2 = \Delta\phi_0/2$.

However, this simplification undesirably limits the design space, which prohibits the network from operating at wideband. Thus, we eliminate this simplification in our work to significantly improve the phase error performance over the frequency band of interest. The phase responses of HP and LP networks, ϕ_{HPN} and ϕ_{LPN}, as a function of frequency f are presented in (5-5) and (5-6), respectively.

$$\phi_{HPN}(f) = \tan^{-1}\left[\frac{f_1}{f}\tan\left(\frac{\phi_1}{2}\right)\frac{1+\cos^2(\phi_1/2)-(f_1/f)^2\sin^2(\phi_1/2)}{1-2(f_1/f)^2\sin^2(\phi_1/2)}\right], \quad (5\text{-}5)$$

$$\phi_{LPN}(f) = \tan^{-1}\left[\frac{f}{f_2}\tan\left(\frac{\phi_2}{2}\right)\frac{1+\cos^2(\phi_2/2)-(f/f_2)^2\sin^2(\phi_2/2)}{1-2(f/f_2)^2\sin^2(\phi_2/2)}\right]. \quad (5\text{-}6)$$

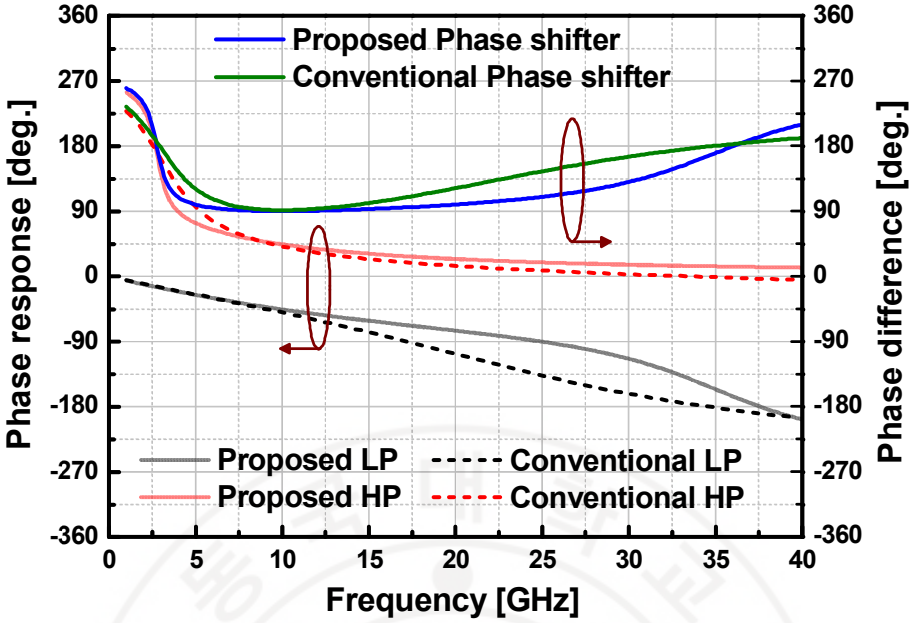


Figure V-3. The demonstration of bandwidth improvement of the proposed method.

A derivative of (5-5) and (5-6) with respect to f represents the slope of the insertion phases of two networks, as expressed in (5-7) and (5-8):

$$\frac{d}{df}\phi_{HPN}(f)= -\frac{f_1}{f^2}\frac{a_1\left[2c_1^2(f_1/f)^4+c_1(2b_1-3)(f_1/f)^2+b_1\right]}{\left[1-2c_1(f_1/f)^2\right]^2+a_1^2(f_1/f)^2\left[b_1-c_1(f_1/f)^2\right]^2}, \tag{5-7}$$

$$\frac{d}{df}\phi_{LPN}(f)= \frac{1}{f_2}\frac{a_2\left[2c_2^2(f/f_2)^4+c_2(2b_2-3)(f/f_2)^2+b_2\right]}{\left[1-2c_2(f/f_2)^2\right]^2+a_2^2(f/f_2)^2\left[b_2-c_2(f/f_2)^2\right]^2}, \tag{5-8}$$

where a_1, b_1, c_1, and a_2, b_2, c_2 are simplified as in

$$a_1 = \tan(\phi_1 / 2); b_1 = 1 + \cos^2(\phi_1 / 2); c_1 = \sin^2(\phi_1 / 2)$$
$$a_2 = \tan(\phi_2 / 2); b_2 = 1 + \cos^2(\phi_2 / 2); c_2 = \sin^2(\phi_2 / 2)$$

To achieve wideband operation of the phase shifter with HP/LP networks, the slope of the phase response of each filter network should be equal and kept constant over the target frequency band. Figure V-3 shows the phase responses of the HP and LP filter network for a 90° phase shift and their corresponding slopes. It can be observed that the slope of the phase response of the HP network is steadier in the high-frequency region about its resonant frequency f_1 whereas that of the LP network is more stable in lower frequency region about its resonant frequency f_2. Thus, to have the minimum phase error over the target frequency band, it is necessary to shift the resonant frequency of the HP network f_1 lower than the center frequency and that of the LP network f_2 higher than f_0. By setting the phase responses of each HP and LP network in opposite directions, we can achieve a flatter phase response slope in the band of interest. With this approach, the phase error is significantly improved within the band. The phase shift of a specific cell is the difference between the two transmission phases as expressed in (5-9). The phase slopes of the two networks at the center frequency f_0 should be aligned to achieve a constant phase shift over a specific frequency range. In other words, the optimized phase error happens when (5-10) and (5-11) are satisfied.

$$\Delta\phi(f) = \phi_{HPN}(f) - \phi_{LPN}(f) \quad (5\text{-}9)$$

$$\Delta\phi(f_0) = \Delta\phi_0 \quad (5\text{-}10)$$

$$\frac{d}{df}\phi_{HPN}(f_0) = \frac{d}{df}\phi_{LPN}(f_0) \quad (5\text{-}11)$$

As can be observed from (5-7) and (5-8), (5-11) naturally happens when setting these constraints: $f_1 f_2 = f_{02}$ and $\phi_1 = -\phi_2$.

Applying the above constraints, (5-9) becomes

$$\Delta\phi_0 = \tan^{-1}$$
$$\left[\frac{f_1}{f_0}\tan\left(\frac{\phi_1}{2}\right)\frac{1+\cos^2(\phi_1/2)-(f_1/f_0)^2\sin^2(\phi_1/2)}{1-2(f_1/f_0)^2\sin^2(\phi_1/2)}\right]-\tan^{-1} \quad (5\text{-}12)$$
$$\left[\frac{f_0}{f_2}\tan(-\phi_1/2)\frac{1+\cos^2(-\phi_1/2)-(f_0/f_2)^2\sin^2(-\phi_1/2)}{1-2(f_0/f_2)^2\sin^2(-\phi_1/2)}\right]$$

The values of ϕ_1 can be obtained by solving the above equation with f_1 and f_2 corresponding to the frequency band of interest. The value of each element in the HP and LP networks can be calculated from (5-1)-(5-4).

The circuit size of HP/LP phase shifters depends on their operating frequency range. For some frequency bands, the above topology and analysis generate impractical inductance and capacitance values. Therefore, it is necessary to employ a different configuration as a realizable solution. One of the candidates uses the BP configuration shown in Figure V-2 as the leading phase network, while the lagging phase network is realized with a third-order LP filter. The transmission phase of the BP network as a function of frequency is expressed in (5-13).

$$\phi_{BPN}(f) = \tan^{-1}\left(\frac{1-af^2}{bf}\right) \quad (5\text{-}13)$$

where $a = 8\pi 2_{L1}C_1 = 1/f_{12}$, $b = 4\pi Z_0 C_1$, and f_1 is the resonant frequency. The derivative of (13) concerning the frequency f is the slope of the transmission phase of the BP network as shown in (5-14) where ϕ_{B0} is the transmission phase at f_0.

$$\frac{d}{df}\phi_{BPN}(f) = \frac{\left[(f_0/f_1)^2-1\right]\left[(f/f_1)^2+1\right]f_0\tan\phi_{B0}}{\left[1-(f_0/f_1)^2\right]^2 f^2+\left[1-(f/f_1)^2\right]^2(f_0\tan\phi_{B0})^2} \quad (5\text{-}14)$$

From the condition $\Delta\phi_0 = \phi_{BPN}(f_0) - \phi_{LPN}(f_0)$, we have (5-15):

$$\phi_{B0} = \tan^{-1}\left[\frac{f_0}{f_2}\tan\left(\frac{\phi_2}{2}\right)\frac{1+\cos^2(\frac{\phi_2}{2})-\frac{f_0^2}{f_2^2}\sin^2(\frac{\phi_2}{2})}{1-2\frac{f_0^2}{f_2^2}\sin^2(\frac{\phi_2}{2})}\right]+\Delta\phi_0 \quad (5\text{-}15)$$

From the condition $d/df\,[\phi_{BPN}(f_0)] = d/df\,[\phi_{LPN}(f_0)]$, we have (5-16):

$$\frac{\left[(f_0/f_1)^2-1\right]\left[(f_0/f_1)^2+1\right]f_0\tan\phi_{B0}}{\left[1-(f_0/f_1)^2\right]^2 f_0^2+\left[1-(f_0/f_1)^2\right]^2(f_0\tan\phi_{B0})^2} = \left(\frac{1}{f_2}\right)\times\frac{2a_2c_2^2(f_0/f_2)^4+a_2c_2(2b_2-3)(f_0/f_2)^2+a_2b_2}{\left[1-2c_2(f_0/f_2)^2\right]^2+a_2^2(f_0/f_2)^2\left[b_2-c_2(f_0/f_2)^2\right]^2}, \quad (5\text{-}16)$$

where $a_2=\tan(\phi_2/2)$, $b_2=1+\cos_2(\phi_2/2)$, and $c_2=\sin_2(\phi_2/2)$.

The value of ϕ_2 can be obtained from (5-15) and (5-16) with f_1 and f_2 as the frequency band of interest. The value of L and C for each network can then be easily calculated. Because the analysis does not take parasitic elements into account for

simplicity, there are errors in the relative phase shift between the calculation and the simulation results.

The basic structures utilized in the proposed wideband phase shifter are third-order HP and LP filters. The phase response of each network is determined by the location of its poles and zeros. Thus, the shape of the phase response of the networks can be manipulated to increase phase error bandwidth by appropriately adjusting the relative location of the poles and zeros. For a qualitative examination, the transfer function of the HP network is expressed in (5-17):

$$S_{21} = \frac{s^3}{\left(s + \frac{1}{Z_0 C}\right)\left(s^2 + \frac{Z_0}{2L}s + \frac{1}{2LC}\right)} \quad (5\text{-}17)$$

The network has a simple pole and a pair of complex poles as follows:

$$p_1 = \frac{1}{Z_0 C} \quad (5\text{-}18.a); \qquad p_{2,3} = -\frac{Z_0}{4L} \pm \frac{1}{2}\sqrt{\frac{Z_0^2}{4L^2} - \frac{2}{LC}} \quad (5\text{-}18.b)$$

Capacitance and inductance values can be calculated at the resonant frequency f_1 given by

$$L_1 = Z_0 / [\omega_1 \sin(\phi_1)] \quad (5\text{-}19)$$

$$C_1 = \left[Z_0 \omega_1 \tan\left(\phi_1 / 2\right) \right]^{-1} \quad (5\text{-}20)$$

Substituting (5-19) and (5-20) into (5-18.a) and (5-18.b) leads to

$$p_1 = \omega_1 \tan\left(\phi_1 / 2\right) \text{ (5-21.a)}; \qquad \left| p_{2,3} \right| = \omega_1 \sin(\phi_1 / 2) \text{ (5-21.b)}$$

Similar results for the LP network can also be obtained as in (5-22).

$$p_1 = \omega_2 / \tan\left(\phi_2 / 2\right) \text{ (5-22.a)}; \qquad \left| p_{2,3} \right| = \omega_2 / \sin(\phi_2 / 2) \text{ (5-22.b)}$$

As can be seen from (5-21) – (5-22), the pole locations are directly proportional to the resonance frequencies of the networks. Thus, when a resonant frequency is shifted, its pole locations move accordingly. If the resonant frequency of the LP network is increased and that of the HP network is decreased, the poles of the LP network will be pushed further apart, and the poles of the HP network will be pulled nearer together on the frequency axis. By doing that, the transition area of the phase responses of the two networks is expanded, resulting in a constant relative phase shift over a broader range of frequency. A phase-shifter with the proposed method is

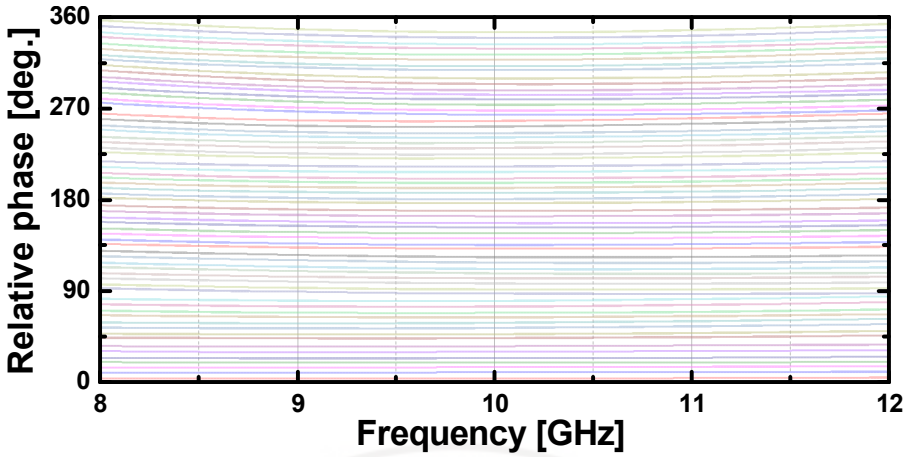


Figure V-4. The simulated relative phase shift levels in all phase states.

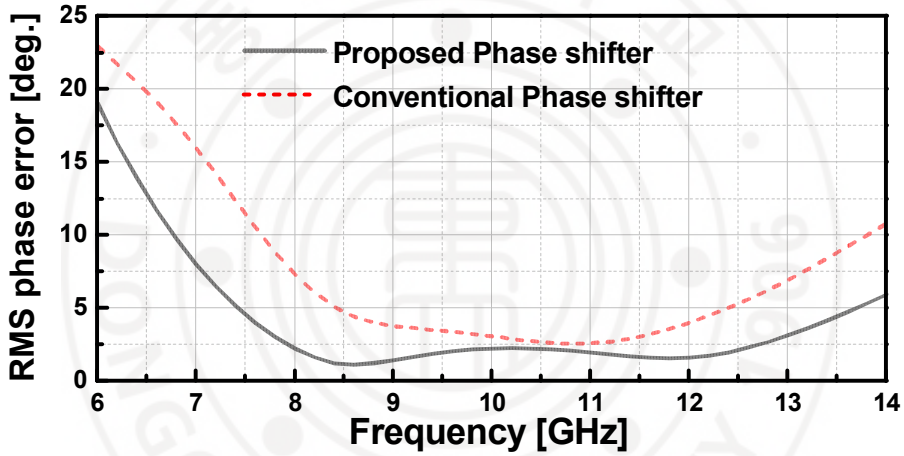
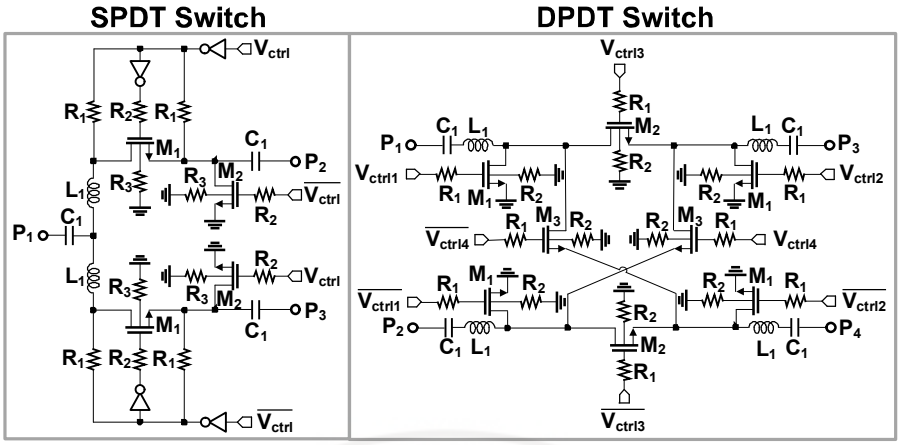


Figure V-5. The simulated RMS phase error of the proposed method and the conventional method.

compared with a conventional one, which illustrates a definite bandwidth improvement as shown in Figure V-3.

The phase-shifting cells for 5.625°, 11.25°, and 22.5° are constructed with a combination of L-C-L BP and T-type LP networks designed with the available sizes of inductances and capacitances. The phase-shifting cell of 45° is constructed with a C-L-C BP and a π-type LP network to minimize its area consumption compared with a T-type network configuration. The phase-shifting cell for 90° comprises a T-type HP filter and a π-type LP filter with third-order filter networks, while 180° phase shifting is formed with two 90° cells in series. Figure V-4 shows the relative phase



Device parameters

M_1	M_2	L_1
130 µm(W) / 60 nm(L)	20 µm(W) / 60 nm(L)	610 pH

C_1	R_1	R_2	R_3
3.2 pF	20 kΩ	14 kΩ	11 kΩ

Device parameters

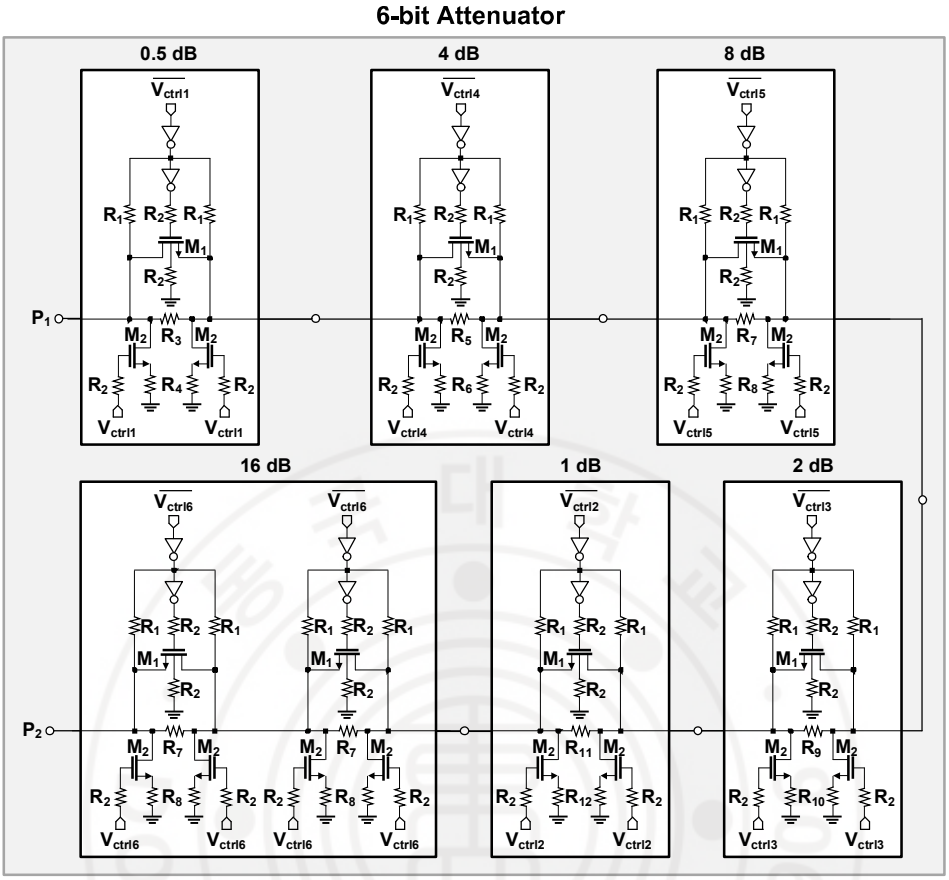
M_1	M_2	M_3
20 µm(W) / 60 nm(L)	130 µm(W) / 60 nm(L)	156 µm(W) / 60 nm(L)

L_1	C_1	R_1	R_2
510 pH	3.2 pF	14 kΩ	11 kΩ

Figure V-6. Schematic [72] and all device parameters of the SPDT (left) and DPDT (right) switches.

shift levels which are very flat over the entire X-band. The RMS phase error is less than 2.3° in 8-12 GHz which is much smaller than that of the conventional design as presented in Figure V-5.

A low loss switching mechanism is required to perform the phase-shifting function with coverage of 360° in steps of 5.625°. The SPDT and DPDT switches configure the path through the phase-shifting elements to produce the desired insertion phase shift. The phase shifter employs two SPDT (single pole double throw) switches and four DPDT (double pole double throw) switches as shown in Figure V-6 [72]. For the SPDT switch, the series transistor (M_1) performs the primary switching function. Shunt transistors (M_2) are added to improve the isolation between different paths. In the design of the SPDT and DPDT switches, the gate terminals are biased through a large resistor R_G to reduce fluctuations of V_{GS}, and V_{GD} due to voltage swings at drain and source. This R_G will keep the on-resistance of the transistors unchanged and avoid excessive voltage across the gate dielectric which causes breakdown issues. The SPDT switch is also used as a duplexer in the proposed transceiver.



Device parameters

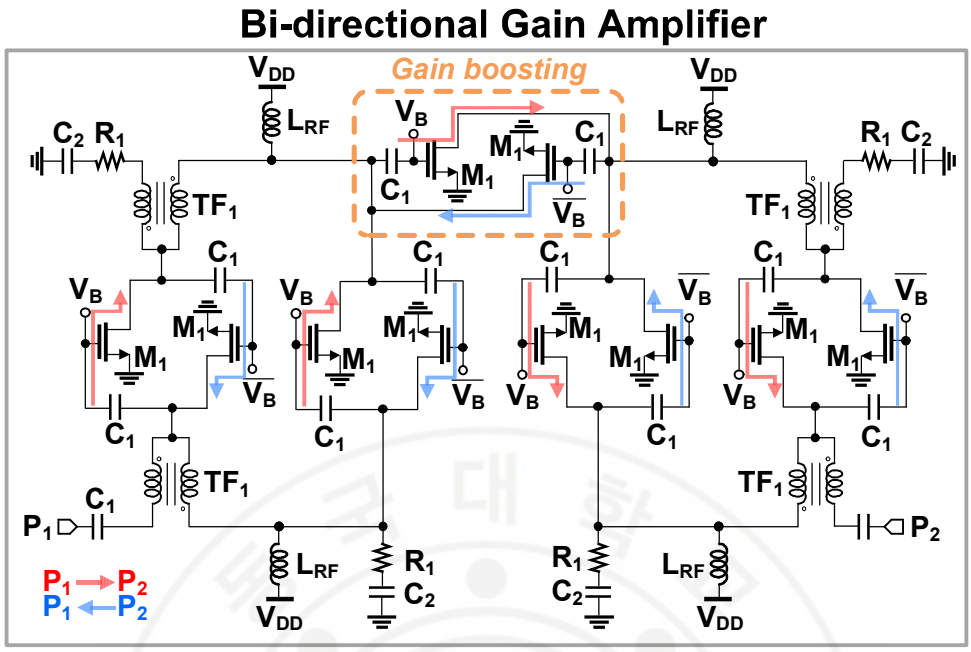
M_1	M_1	R_1	R_2	R_3	R_4	R_5
130 µm(W) / 60 nm(L)	130 µm(W) / 60 nm(L)	20.2 kΩ	13.8 kΩ	6.7 Ω	9.1 kΩ	31 Ω
R_6	R_7	R_8	R_9	R_{10}	R_{11}	R_{12}
82.5 Ω	78.5 Ω	33.5 Ω	21.7 Ω	372.4 Ω	15.2 Ω	3 kΩ

Figure V-7. Schematic and all device parameters of the designed X-band 6-bit step attenuator.

5.2.2. 6-bit step attenuator

There are two basic topologies commonly employed in the digital attenuator designs: resistive π-type attenuators, and resistive T-type attenuators. These conventional structures consist of series/shunt switches and resistors. The switches are usually realized as a single NMOS transistor, so NMOS transistors are crucial elements in determining the performance of a digital step attenuator. Explicitly, NMOS switches can be approximately modeled by the resistor R_{ON} in the ON state and the capacitor C_{OFF} in the OFF state.

In this design, a 6-bit CMOS digital attenuator is designed with a resistive π-type structure as depicted in Figure V-7. It should be noted that the implementation of the 6-bit step attenuator was co-worked with Mr. Nguyen [77-78]. The attenuator covers the range of 0 to 31.5 dB with steps of 0.5 dB. The relative attenuation level is obtained by taking the difference between the attenuation state and the thru state as controlled by single NMOS switches. One of the challenges in designing an attenuator is to sustain reasonable impedance matching for both of its states. The large resistor R_2 at the gate keeps V_{GS} and V_{GD} almost the same during its operation, which relieves the impedance changes that depend on the switch states. By using two inverters with large resistors to bias source and drain terminals of the series switch, the contrast of the channel resistance of the series switch (M_1) for ON/OFF states can be improved to provide less insertion loss of the attenuator at the thru state than that of the attenuators in [70-72].



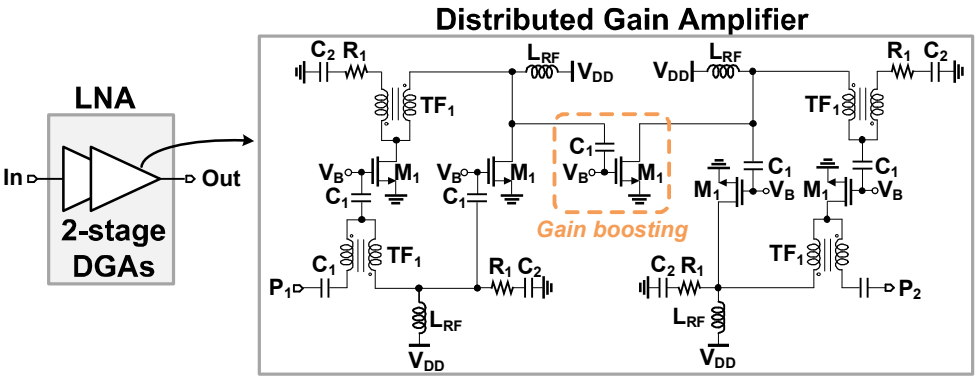
Device parameters

M_1	TF_1	L_{RF}	C_1	C_2	R_1
60 µm(W) / 60 nm(L)	720 pH	800 pH	815 fF	3.2 pF	50 Ω

Figure V-8. Schematic and all device parameters of the transformer-based BDGA.

5.2.3. Cascaded distributed amplifiers

Distributed gain amplifiers (DGA) have been widely used in wideband applications in the microwave regime due to their excellent input and output matching characteristics as well as their wideband frequency response [80-81]. However, the summing nature of the distributed amplifier cells results in a power gain limitation, which is typically less than 10 dB. A wideband low-noise amplifier (LNA) and bi-directional gain amplifiers (BDGAs) composed of cascading distributed amplifiers with a common source (CS) stage in the middle were used to provide higher power gain as illustrated in Figures V-8 and V-9. Furthermore, a transformer was used to reduce area occupancy, minimizing the number of inductors used for the artificial transmission line by combining the parasitic capacitance of the DGA transistors.



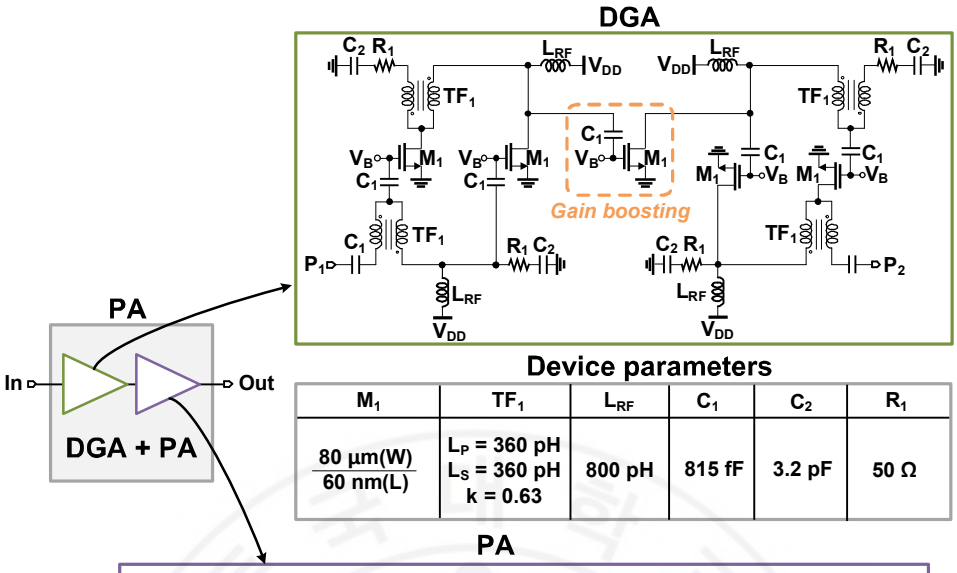
Device parameters

M_1	TF_1	L_{RF}	C_1	C_2	R_1
80 µm(W) / 60 nm(L)	L_P = 360 pH L_S = 360 pH k = 0.63	800 pH	815 fF	3.2 pF	50 Ω

Figure V-9. Schematic and all device parameters of the transformer-based LNA.

The schematic diagram for the BDGA is presented in Figure V-8. The circuit is composed of four-stage bi-directional distributed gain amplifiers (BDGAs) and a cascading connection stage for gain-boosting at the middle. Like the conventional BDGA, on-chip transformers and the parasitic capacitance of transistors form artificial transmission lines at the input and output, enabling the amplifier's broadband operation. Because of the cascading connection between the BGA stages, the cascaded BDGA takes advantage of multiplicative gains.

The schematic and the device parameters for the LNA are presented in Figure V-9. The LNA consists of gain amplifiers (GAs) and the cascading connection stage for gain-boosting in the middle. It is noteworthy that the center frequency of the LNA is around 12 GHz since the phase shifter has quite a large amount of insertion loss at this frequency. In other words, the LNA is designed to compensate for the loss in the whole transceiver at that frequency.



M_1	TF_1	L_{RF}	C_1	C_2	R_1
80 µm(W) / 60 nm(L)	L_P = 360 pH L_S = 360 pH k = 0.63	800 pH	815 fF	3.2 pF	50 Ω

M_2	M_3	TF_2	TF_3	TF_4
250 µm(W) / 60 nm(L)	1200 µm(W) / 60 nm(L)	L_P = 390 pH L_S = 1.19 nH k = 0.68	L_P = 370 pH L_S = 300 pH k = 0.67	L_P = 130 pH L_S = 450 pH k = 0.65

R_2	R_3	R_4	C_3	C_4	C_5	C_6	C_7	C_8
300 Ω	300 Ω	600 Ω	500 fF	530 fF	500 fF	530 fF	530 fF	282 fF

Figure V-10. Schematic and all device parameter of the full X-band PA.

5.2.4. Wideband power amplifier

The wideband PA was employed after the SPDT duplexer for Tx operation to enhance the output power and provide a proper power gain of the transmitter as shown in Figure V-10. The implementation of the wide-band power amplifier was contributed by Mr. Van-Son Trinh based on his previous work in [82].

The PA is constructed from two stages of push-pull amplifiers using a cascode configuration combined with two stages of a transformer-based distributed amplifier [77]. The push-pull structure naturally delivers the combined power of two independent transistors to the load. Moreover, by using a 1:2 transformer at the output, the load impedance seen by the transistors could be effectively reduced [82].

Therefore, more current can be drawn by the transistor, which results in higher output power delivered to the load. In this design, an RC bias circuit which is similar to the bias configuration used for a stacked transistor in SOI-CMOS technology [83-84] is employed to bias the gate of the cascode transistor M_3 to achieve equally distributed voltage over the two stacked NMOSs in the cascade configuration. An RC feedback network is also used to make the PA stable with its improved bandwidth [85].

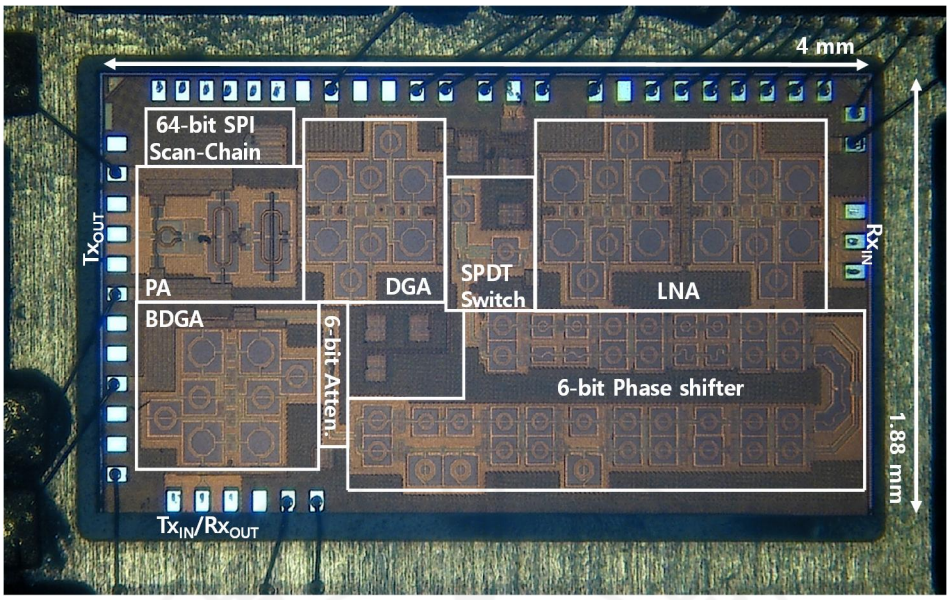


Figure V-11. Chip-photograph of the fabricated X-band phased-array transceiver in 65-nm CMOS technology.

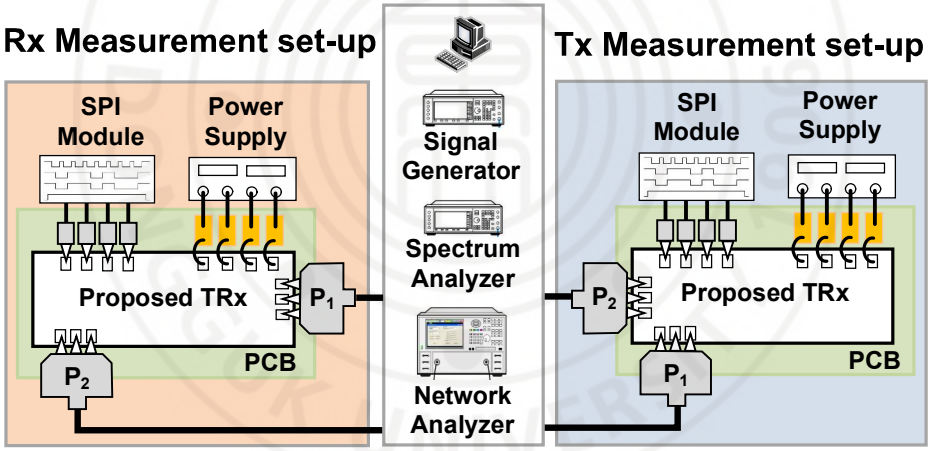


Figure V-12. The measurement setup for the S-parameters, phase shift, attenuation, and output power of the chip in Rx/Tx operation.

5.3. Measurement results

The X-band phased-array TRM chip was fabricated in 65- nm CMOS technology. Figure V-11 shows the chip-photograph of the implemented transceiver, which occupies 4 mm ×1.88 mm, including all the pads. As shown in Figure V-12, the TRM chip was measured with on-chip probing. A 64-bit serial-peripheral-interface (SPI) scan-chain was integrated for digital control of each block. The equipment used for

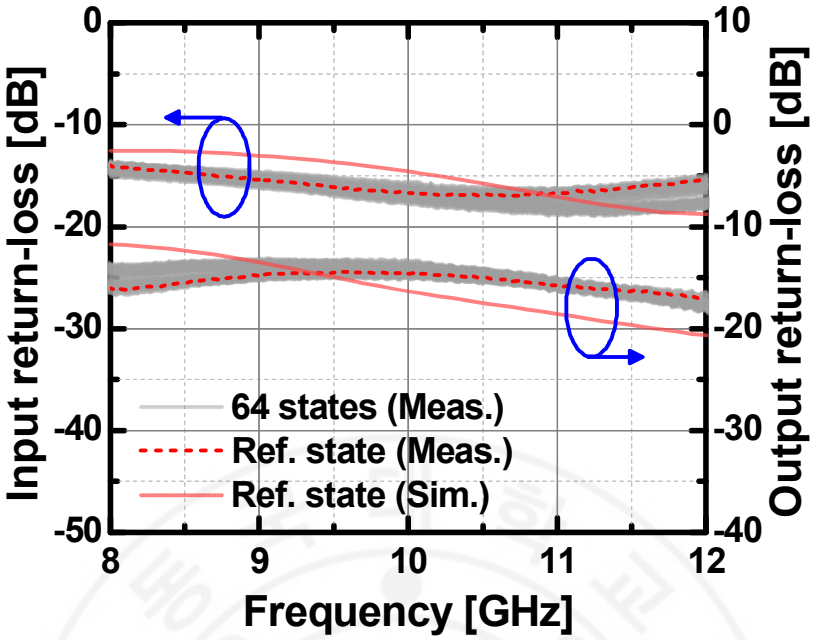


Figure V-13. Simulated and measured results for the S_{11} and S_{22} of the transceiver in Tx operation depending on 64 different phase-shift states.

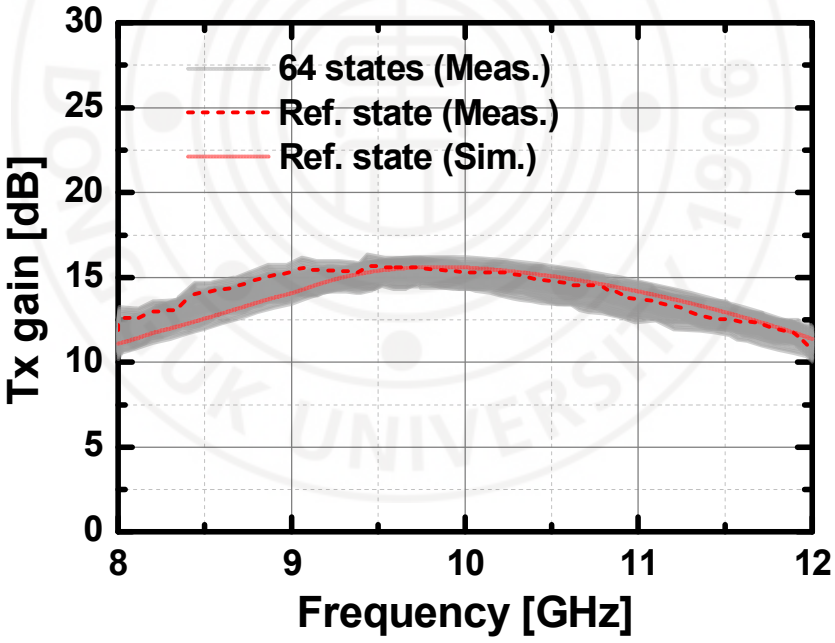


Figure V-14. Simulated and measured results for the Tx gain of the transceiver in Tx operation depending on 64 different phase-shift states.

measurement was as follows: Agilent E4407B spectrum analyzer, Keysight DSO-X 6002A digital oscilloscope, Agilent 83623B signal generator, and Keysight N5224A network analyzer.

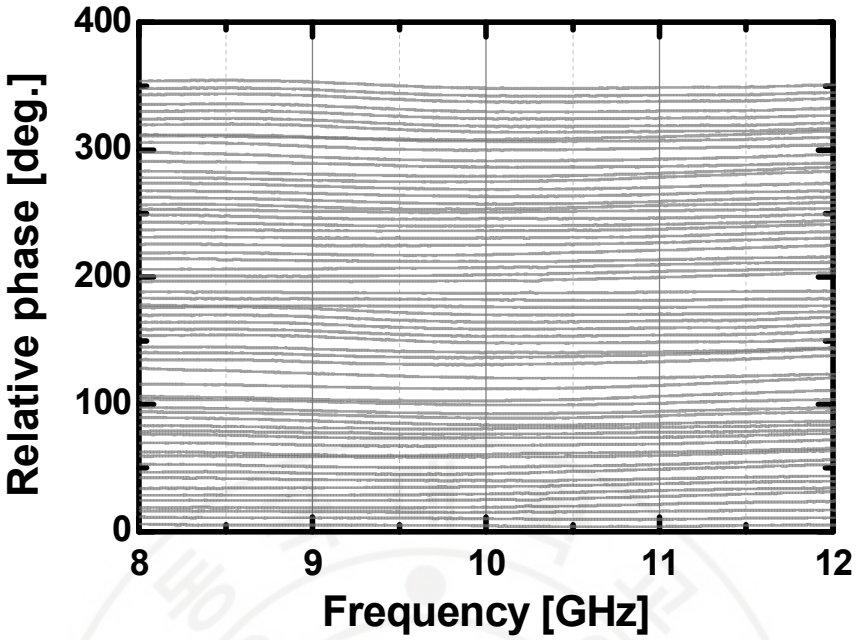


Figure V-15. Measured relative phase shift of the transceiver in Tx operation.

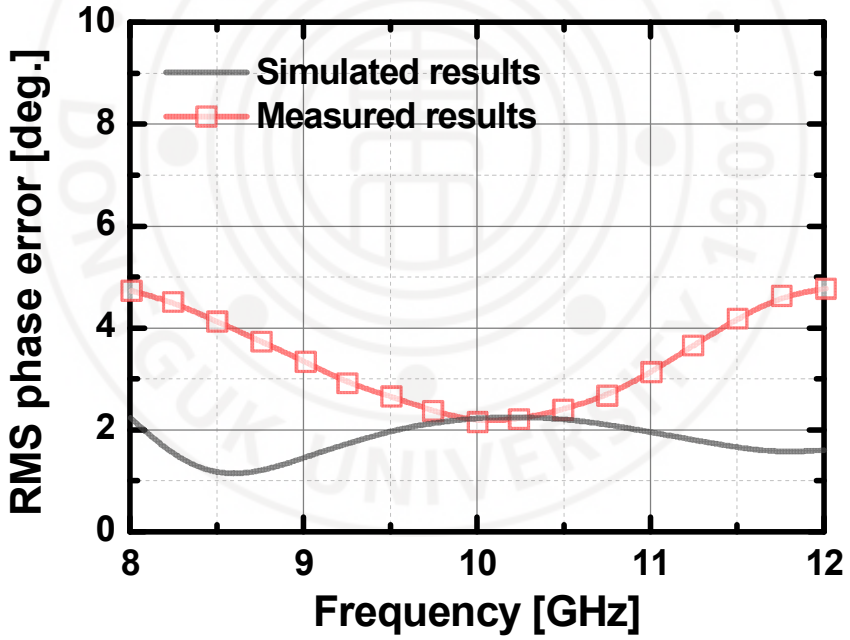


Figure V-16. Simulated and measured results for the RMS phase error of the transceiver in Tx operation.

In Tx mode, the simulated and measured S_{11} and S_{22} for 64 different phase states are presented in Figure V-13. Between 8 and 12 GHz, the input and output return losses are better than 10 dB. Figure V-14 shows the simulated and measured gain of the Tx for 64 different phase states. The gain flatness is about ± 2 dB. As shown in

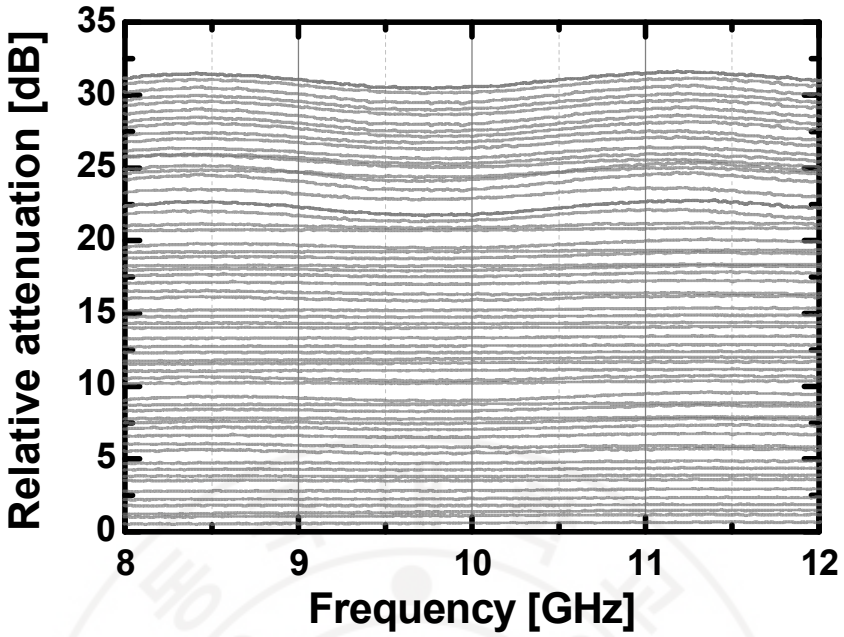


Figure V-17. Measured relative attenuation level of the transceiver in Tx operation.

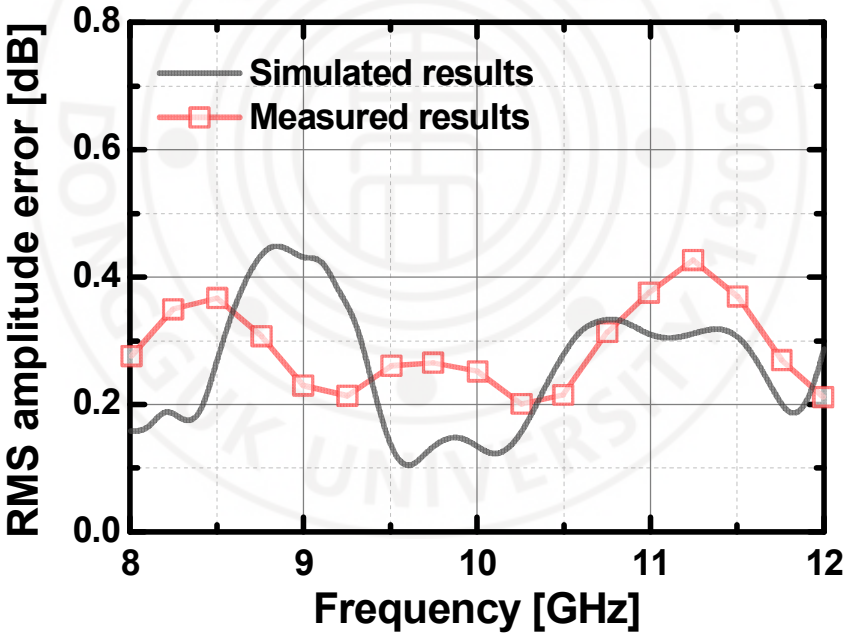


Figure V-18. Simulated and measured results for the RMS amplitude error of the transceiver in Tx operation.

Figure V-15, the measured relative phase-shift in the X-band has a resolution of 5.625° and covers 0° to 360°. The simulated and measured results for the RMS phase error in the X-band are depicted in Figure V-16. The measured RMS phase error is less than 5°, which is smaller than the resolution. The measured relative attenuation

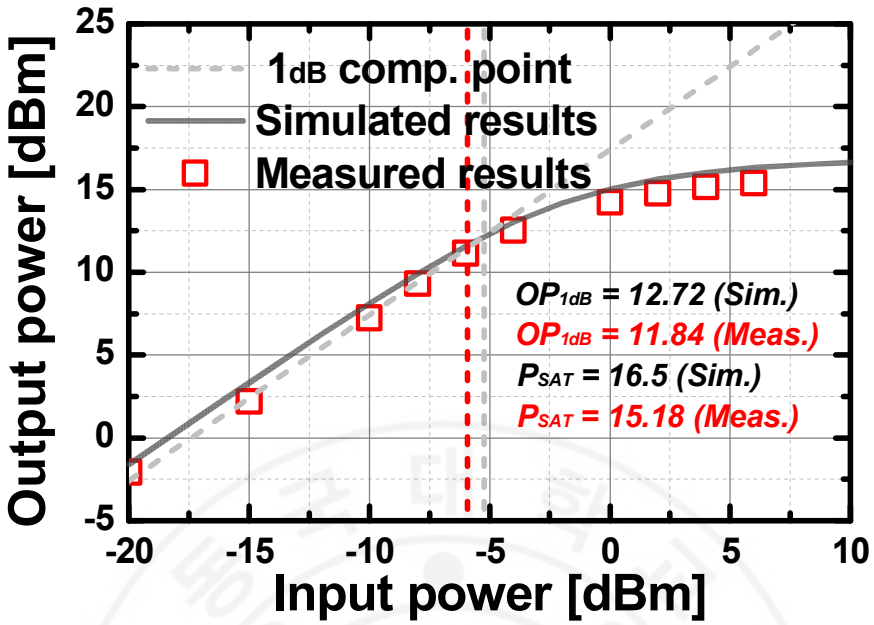


Figure V-19. Simulated and measured results for the output power of the transceiver in Tx operation at 10 GHz.

level of the transceiver in the Tx operation is shown in Figure 17. It shows a resolution of 0.5 dB in the whole X-band. The simulated and measured results for the RMS amplitude error of the transceiver in the Tx operation are illustrated in Figure V-18. In full X-band, the measured RMS amplitude error is less than 0.45 dB, which is smaller than the amplitude resolution. Figure V-19 shows the output power response of the transceiver in Tx operation measured with a 10-GHz input signal at the reference state of the phase shifter (i.e., all zero-bit state). The saturated output power (P_{SAT}) of 15.18 dBm and output 1-dB compression point (OP_{1dB}) of 11.84 dBm can be o bserved. The total power consumption of the transceiver with 1 V supply is 216 mW at the OP1dB output point.

In Rx mode, the simulated and measured S_{11} and S_{22} for 64 different phase states are shown in Figure V-20. The input and output return losses are better than 10 dB. Figure V-21 illustrates the simulated and measured gain of the Rx depending on 64 different phase states. The gain flatness is about ± 2 dB, and the 3-dB bandwidth is wider than 5.2 GHz (7 to 12.2 GHz). As shown in Figure V-22, the measured relative

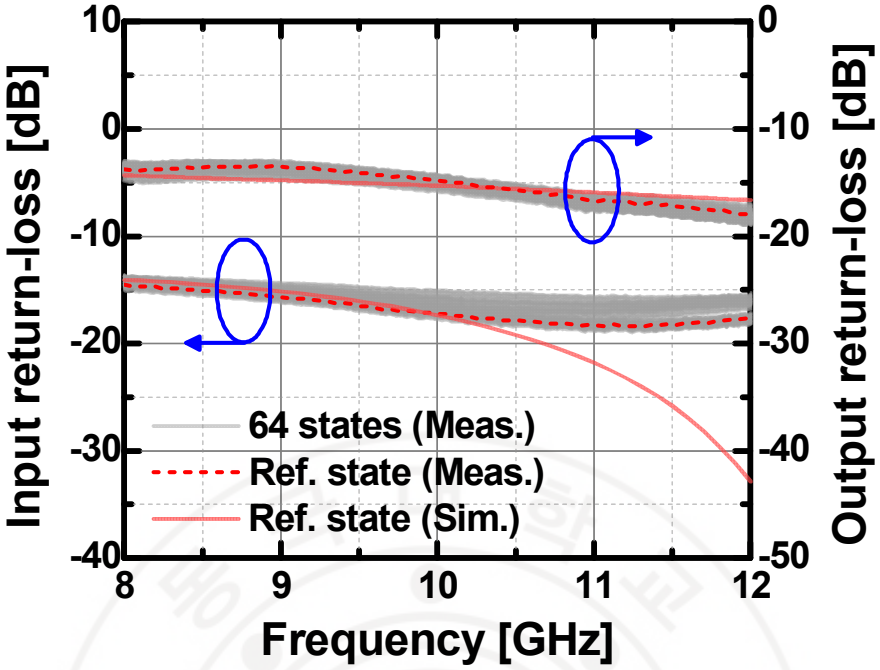


Figure V-20. Simulated and measured results for the S_{11} and S_{22} of the transceiver in Rx operation depending on 64 different phase-shift states.

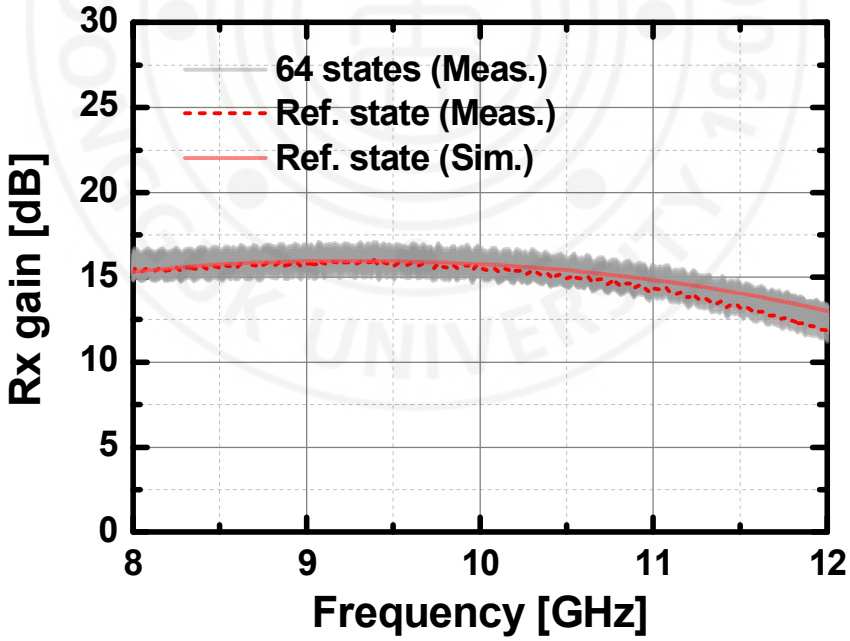


Figure V-21. Simulated and measured results for the Rx gain of the transceiver in Rx operation depending on 64 different phase-shift states.

phase-shift in the X-band has a resolution of 5.625° and covers 0° to 360°. The simulated and measured results for the RMS phase error in the X-band are depicted

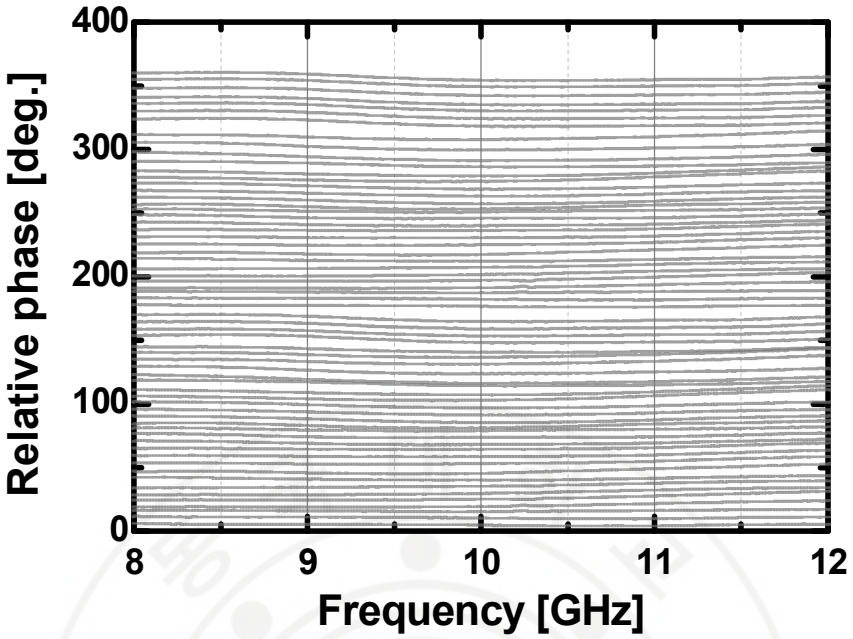


Figure V-22. Measured relative phase shift of the transceiver in Rx operation.

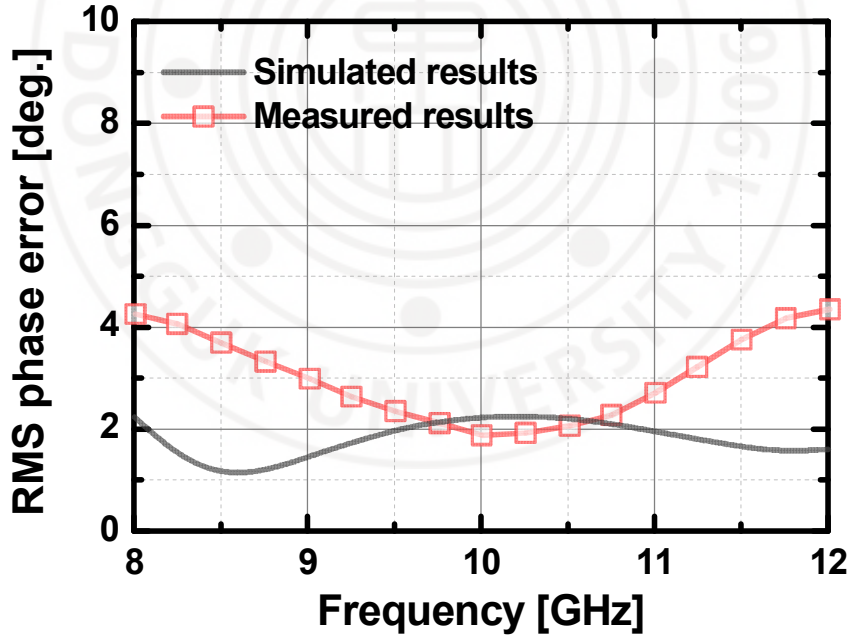


Figure V-23. Simulated and measured results for the RMS phase error of the transceiver in Rx operation.

in Figure V-23. The simulated and measured RMS phase error is less than 5°, which is smaller than the resolution. The measured relative attenuation level of the transceiver in the Rx operation is shown in Figure V-24. It shows a resolution of 0.5

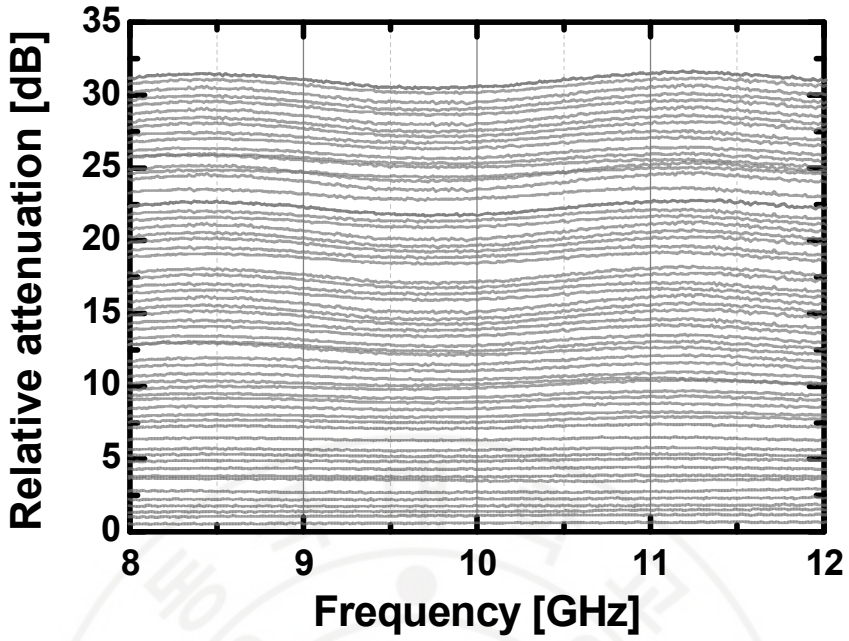


Figure V-24. Measured relative attenuation level of the transceiver in Rx operation.

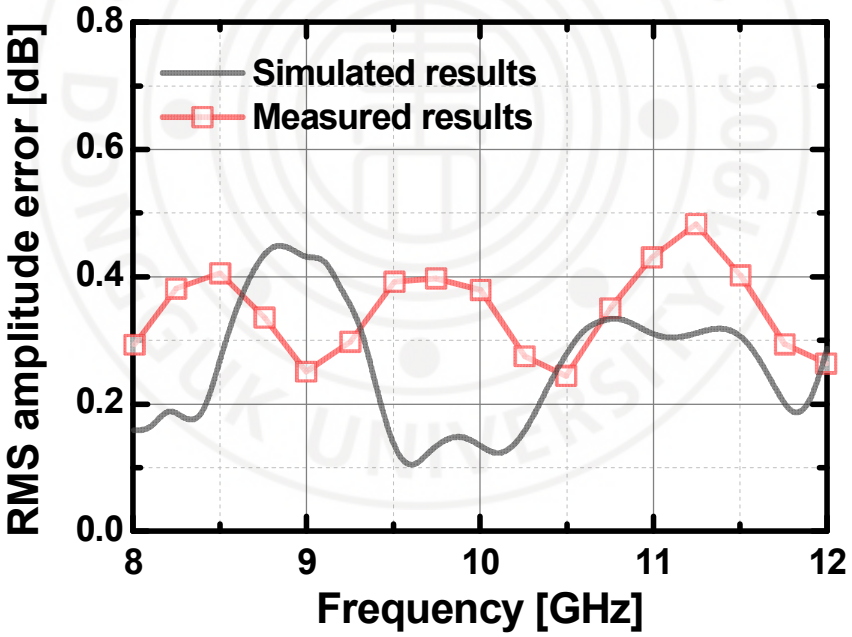


Figure V-25. Simulated and measured results for the RMS amplitude error of the transceiver in Rx operation.

dB in the X-band. The simulated and measured RMS amplitude error of the transceiver in the Rx operation is illustrated in Figure V-25. In full X-band, the measured RMS amplitude error is less than 0.45 dB which is smaller than the

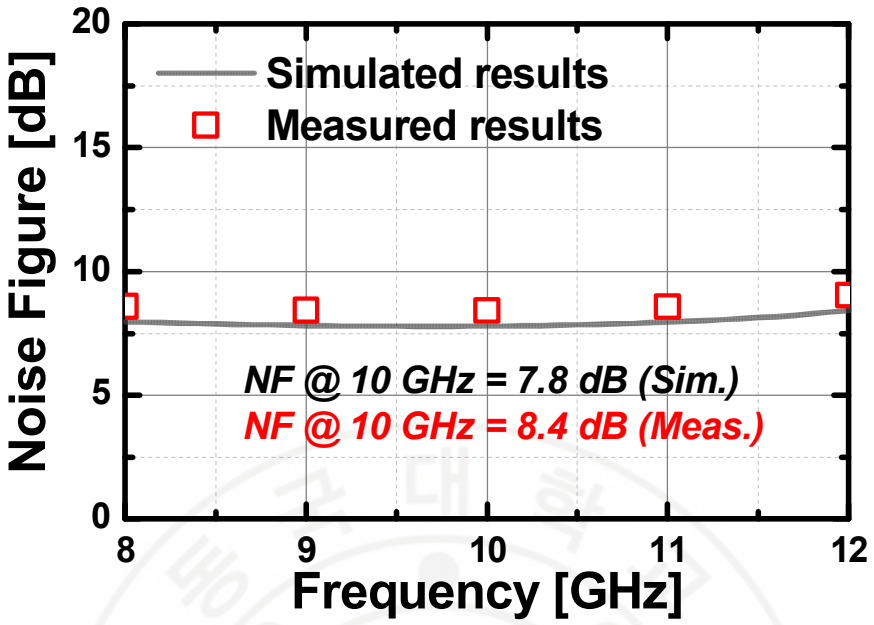


Figure V-26. Simulated and measured NF of the transceiver in Rx operation.

resolution. The simulated and measured noise figure (NF) of the transceiver in the Rx operation is presented in Figure V-26. The NF measurement was carried out from the Y-factor method, showing a minimum NF of 8.4 dB in the w hole X-band.

Table V-1 compares the implemented transceiver with previously published III-V chipsets and SiGe based transceivers for X-band phased-array systems. It shows that the implemented TRM chip shows the highest OP1dB, gain, and widest operating frequency range among the CMOS based phased-array chips and has RF performance comparable with SiGe transceivers and III-V chipsets with much lower power consumption.

Table V-1. Comparison with previously reported state-of-the-art X-band phased-array transceivers.

Ref.	Tech.	f_{RF} [GHz]	PS /Atten. # of bits	Func.	Rx NF [dB]	Rx/Tx Gain [dB]	Rx/Tx OP_{1dB} [dBm]	RMS phase/ amp. error [dB]	Chip area [mm^2]	Rx/Tx P_{DC} [mW]
This work	65nm CMOS	8-12	6/6	Rx /Tx	8.4	15 /15	NA /11.84	5/0.45	7.52	110 /216
[58]	0.2µm HEMT	9-12	7/7	Rx /Tx	8	5 /5	NA /14	1.5 /0.08	18.48	600 /600
[59]	0.25µm HEMT	8.5-11.5	6/5	Rx /Tx	2.3	27 /NA	13 /19	NA/5.5	20	1200 /1200
[60]	0.25µm SiGe	8-11	5/5	Rx /Tx	9	20 /30	NA /18	6/1.5	8.4	1500 /1500
[61]	0.25µm SiGe	8-11	5/5	Rx /Tx	10	17 /17	NA /12	6/2	16	800 /800
[62]	0.18µm SiGe	6-18	4/NA	Rx	4.2	24.5 /NA	NA /NA	5.7/0.9	5.39	561 /NA
[63]	0.13µm SiGe	8-10.7	5/NA	Rx	4.1	11 /NA	12.5 /NA	9/0.6	13.3	33 /NA
[64]	0.13µm SiGe	9-11	5/NA	Rx /Tx	3	25 /22	6 /28	3.8/1.2	15.6	352 /4128
[65]	0.25µm SiGe	8-12	6/6	Rx /Tx	9.8	17.8 /17.7	NA /17	2/0.25	9	330 /792
[66]	0.18µm SiGe	8-16	7/7	Rx /Tx	10	16 /21	NA /8.5	2.8/0.3	16	215 /280
[67]	0.13µm SiGe	8-12	6/6	Rx /Tx	11.5	13 /NA	NA /12	3/0.5	54	NA
[68]	0.13µm SiGe	8.5-10.5	5/NA	Rx	3.4	12.2 /NA	-7.5 /NA	12/0.4	7.25	144 /NA
[69]	0.18µm SiGe	8.5-10	6/6	Rx /Tx	8.5	12 /11	11 /11.5	2/0.25	12.8	670 /640
[70]	0.13µm SiGe	8.5-10.5	6/5	Rx /Tx	7.5	3.5 /3.5	6.5 /6.5	4.3/0.8	1.2	154 /154
[71]	0.13µm SiGe	7.9-9.6	4/3	Tx	NA	NA /11.5	NA /8.8	5/0.5	8.7	870 /870
[72]	65nm CMOS	8-10.5	6/6	Rx /Tx	10	3.7 /3.7	NA /5.1	4/0.5	9.56	170 /170
[73]	0.13µm CMOS	9-10	6/5	Rx /Tx	NA	9 /12	NA /11	2.3/0.4	2.8	500 /800

VI. W-Band Divide-by-Three Injection-Locked Frequency Divider With Injection Current Boosting Utilizing Inductive Feedback

6.1. Introduction

Agile and wideband signal generator using a phased locked loop (PLL) is essential for a highly integrated millimeter-wave (mm-wave) transceiver. Specifically, the first-stage frequency divider in a W-band PLL is one of the critical components since the operation frequency of a divider in the PLL must cover the whole oscillation frequency of a voltage controlled oscillator (VCO) with a reasonable input power level. For the mm-wave application, the static/dynamic current-mode logic (CML) based frequency dividers (FDs) [86-88], and the injection locked frequency dividers (ILFDs) are typically employed for the first-stage of the divider chain in the feedback-loop [89-98]. Although static CML based FD can achieve wide bandwidth, they consume higher power dissipation than dynamic CML FDs and ILFDs for a specific operating frequency. Moreover, ILFD can be applicable to even higher frequency than static CML FD owing to the injection-locking mechanism [89]. Thus, the ILFD is one of the most promising solutions to achieve an ultra-high operating frequency with low power consumption. Among many types of ILFDs, the inductance-capacitance (LC) based divide-by-three ILFDs are suitable for W-band applications due to high division ratio as well as their low power dissipation [90-95]. Figure VI-1 presents the mechanism of the conventional divide-by-three ILFD [90]. The injection current transformed by the injection voltage of the input transistor is applied to the mixer1 where the third harmonics of the injection current is mixed with the second harmonic so that it can be locked by the one-third of the applied input frequency (f_{in}). One of the critical disadvantages of the ILFD is the narrow locking range at the expense of low power consumption. The locking range of divide-by-three ILFD is given by [89]:

$$LR = \frac{I_{Inj}}{Q_R \times I_{osc}} \qquad (6\text{-}1)$$

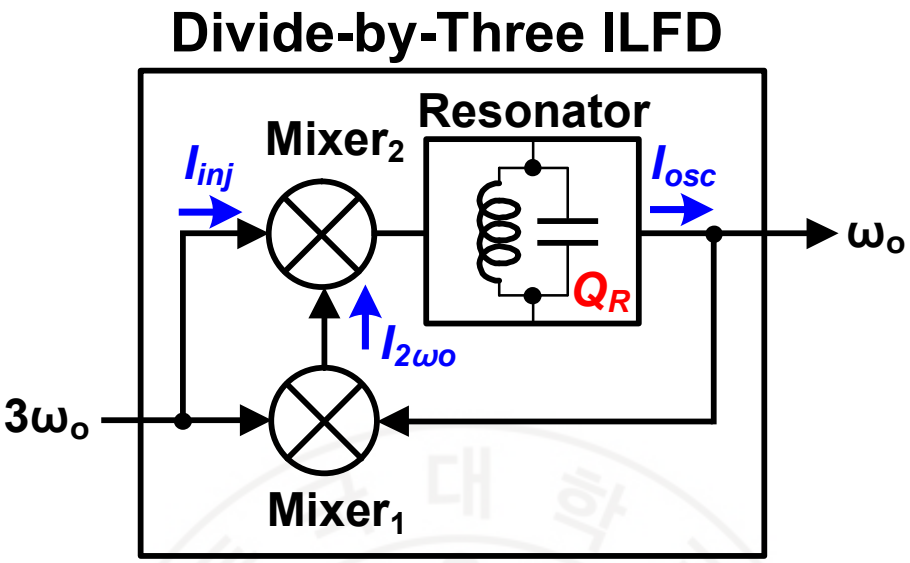


Figure VI-1. A block diagram of the function of divide-by-three injection locked frequency divider (ILFD).

where I_{inj} is the injection current from the input transistor, I_{osc} is the oscillation drain current of the mixer, and QR is the quality factor of the resonator used in the ILFD. To improve the locking range of the divide-by-three ILFD in the mm-wave regime, a variety of studies have been conducted. In [93], an injection enhancement with resistive feedback was applied, but its locking range without the varactor was still narrow which is less than 3.8%. In [95], a second harmonic generator was proposed to enhance the strength of the weak harmonic component, but it was at the expense of more power dissipation.

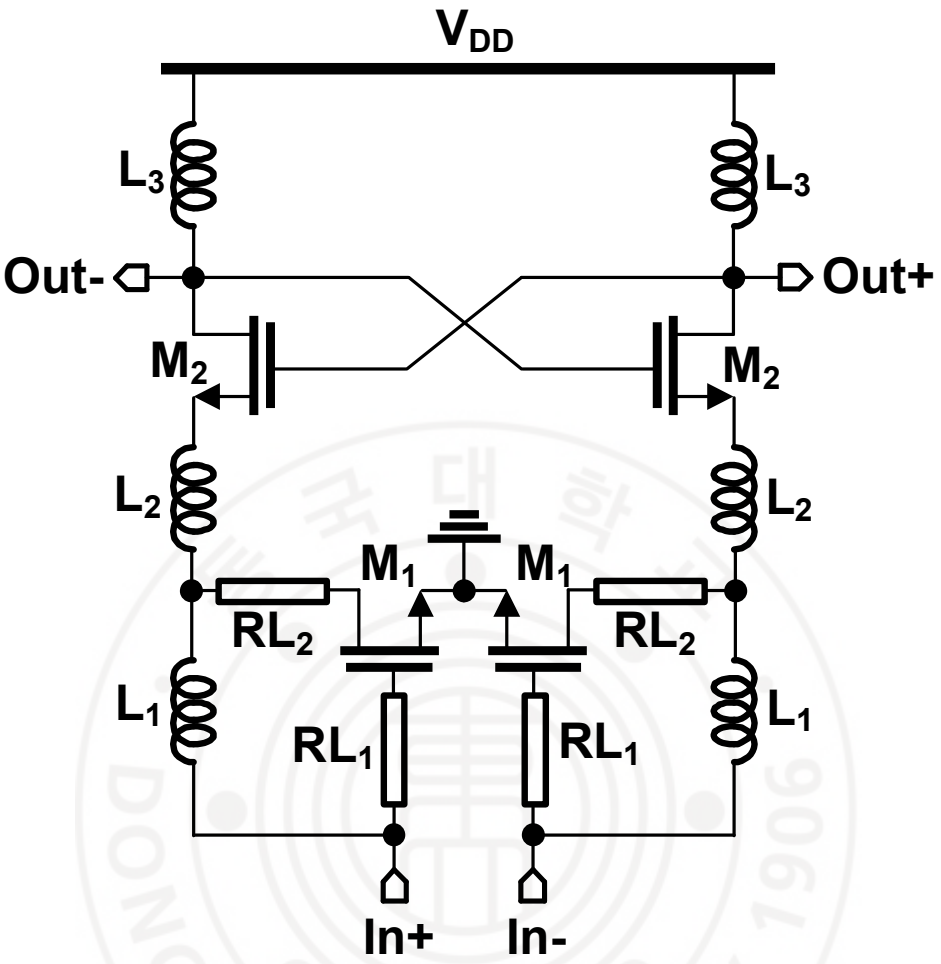


Figure VI-2. Schematic of the proposed ILFD with inductive feedback for I_{inj} boosting [102].

6.2. Design of the ILFD with inductive feedback

The schematic diagram of the proposed ILFD is shown in Figure VI-2 [102]. The ILFD consists of an injector M_1 to convert the input voltage into injection current, a transistor M_1 as $Mixer_1$, the cross-coupled pair as $Mixer_2$, a shunt LC tank consisting of L_3 and the parasitic capacitance from M_2 working as a band-pass filter, two routing lines (RL_1 and RL_2), and two lumped inductors (L_1 and L_2). Specifically, L_1 is employed as the inductive feedback component to enhance the injection efficiency of the $2\omega_o$ and $3\omega_o$ components, and L_2 is used as the peaking inductor to boost the voltage swing at the source node of M_2 [99-100].

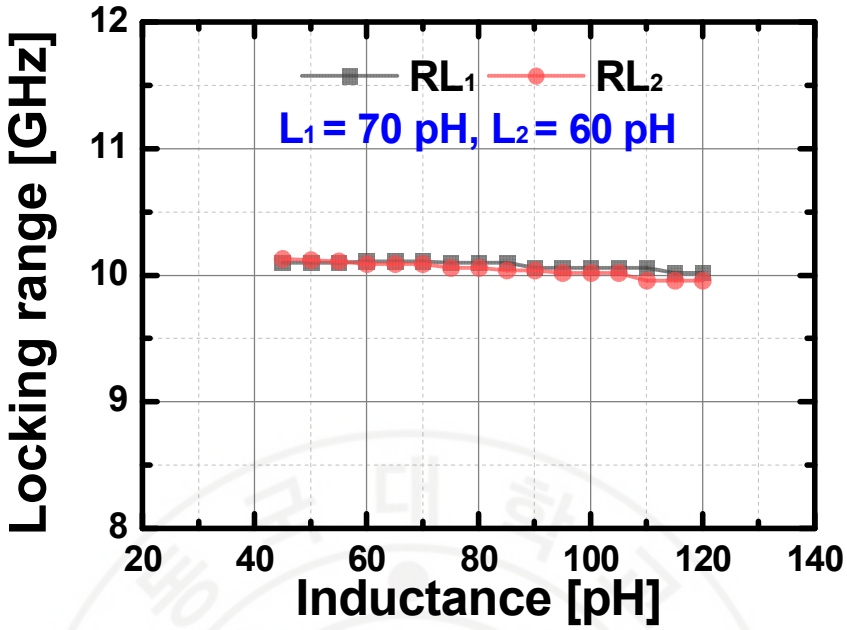


Figure VI-3. Locking range *versus* RL_1 and RL_2 with given L_1=70pH and L_2=60pH.

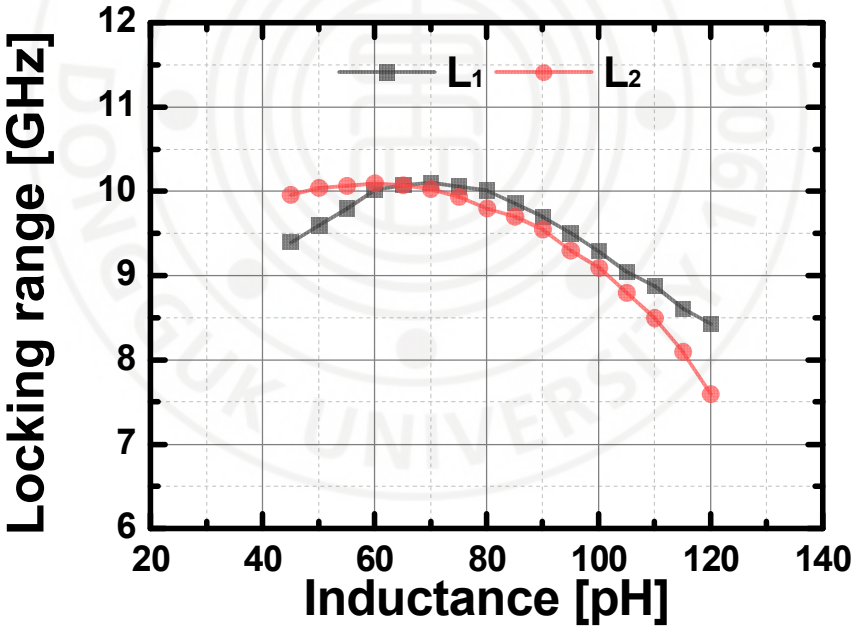


Figure VI-4. Locking range *versus* L_1 and L_2.

To maximize the locking range of the proposed divider, the values of L_1 and L_2 have been swept, and the locking range is strongly affected by the size of L_1 and L_2 as denoted in Figures VI-3 and VI-4. This verifies that the line inductances from the

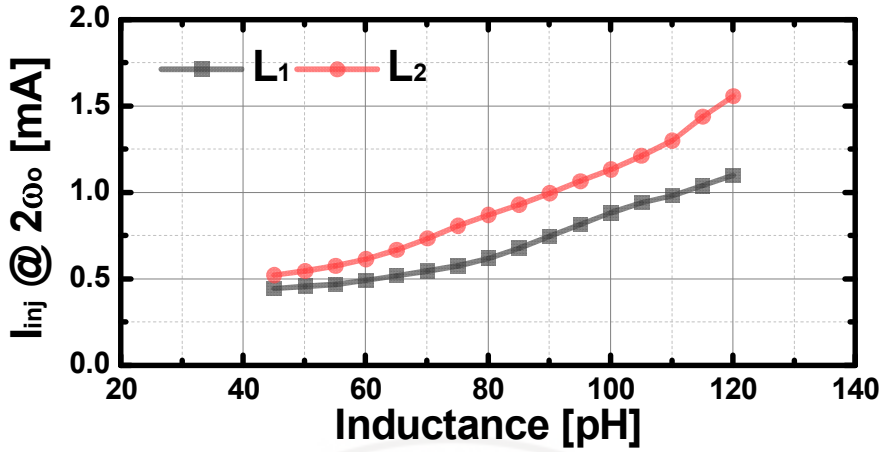


Figure VI-5. Injection current at $2\omega_o$ *versus* L_1 and L_2.

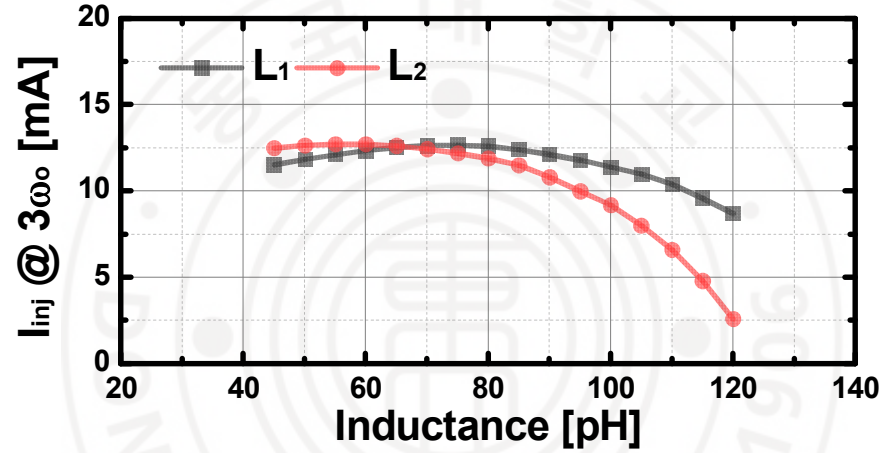


Figure VI-6. Injection current at $3\omega_o$ *versus* L_1 and L_2.

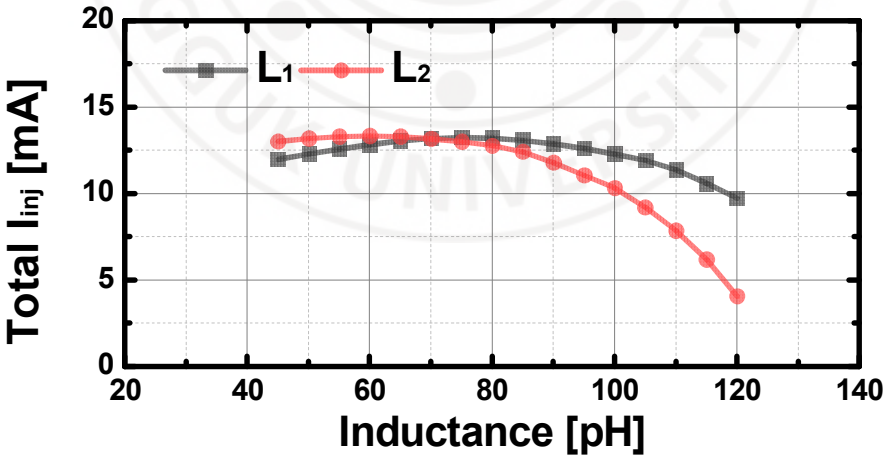


Figure VI-7. Total ($I_{2\omega o}$+$I_{3\omega o}$) injection current *versus* L_1 and L_2.

extra routing lines are not sensitive to the locking range up to 100pH. Figures VI-5, VI-6, and VI-7 depict the source injection current (I_{inj}) of M_2 with the $2\omega_o$ and $3\omega_o$

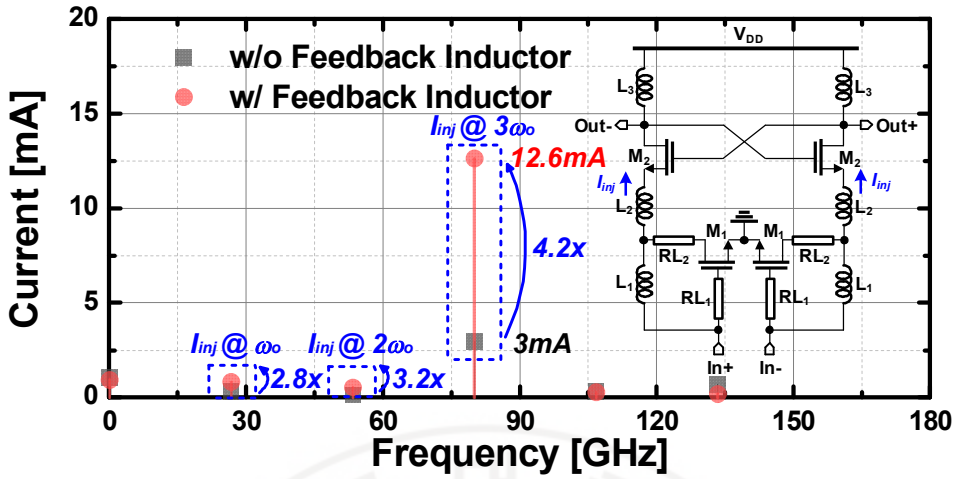


Figure VI-8. Simulated injection current with and without feedback inductor for the proposed ILFD.

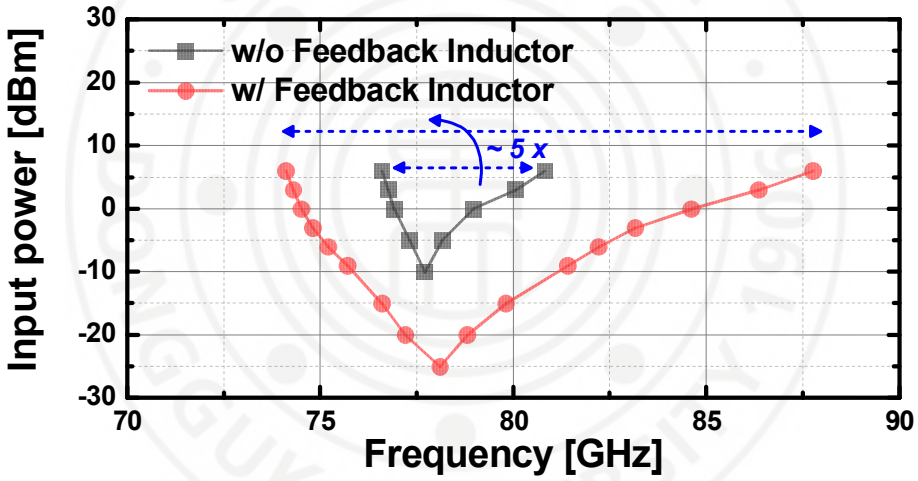


Figure VI-9. Simulated locking range with and without feedback inductor for the proposed ILFD.

components depending on the size of L_1 and L_2.

We emphasize that the injection efficiency is proportional to the injection current [101]. Figure VI-8 compares the simulation results of the I_{inj} with and without L_1=70pH and L_2=60pH. With the optimized size of the inductors, the $2\omega_o$ and $3\omega_o$ components were improved by 3.2 and 4.2 times, respectively. As a result, the locking range of the proposed ILFD with the input power of 0dBm is from 74.5GHz to 84.6GHz, as presented in Figure VI-9.

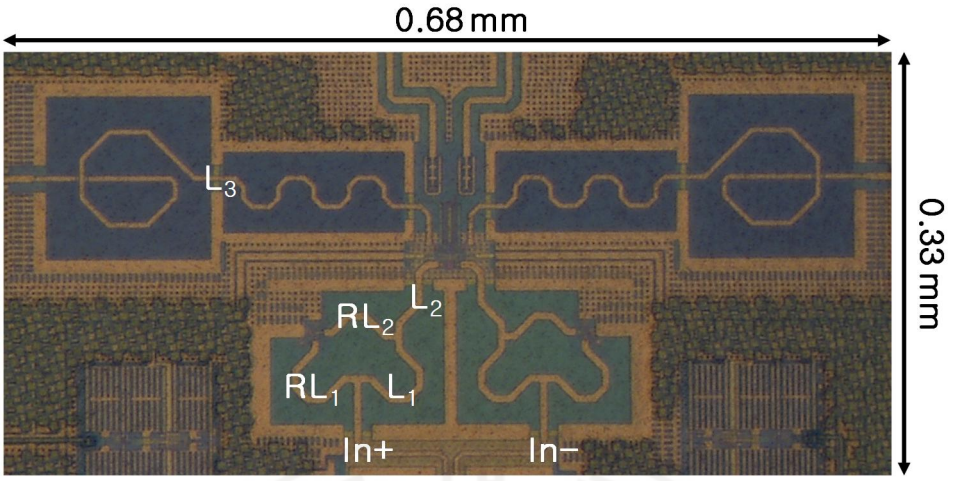


Figure VI-10. A microphotograph of the proposed ILFD chip with the inductive feedback (core size: 0.68 x 0.33 mm^2).

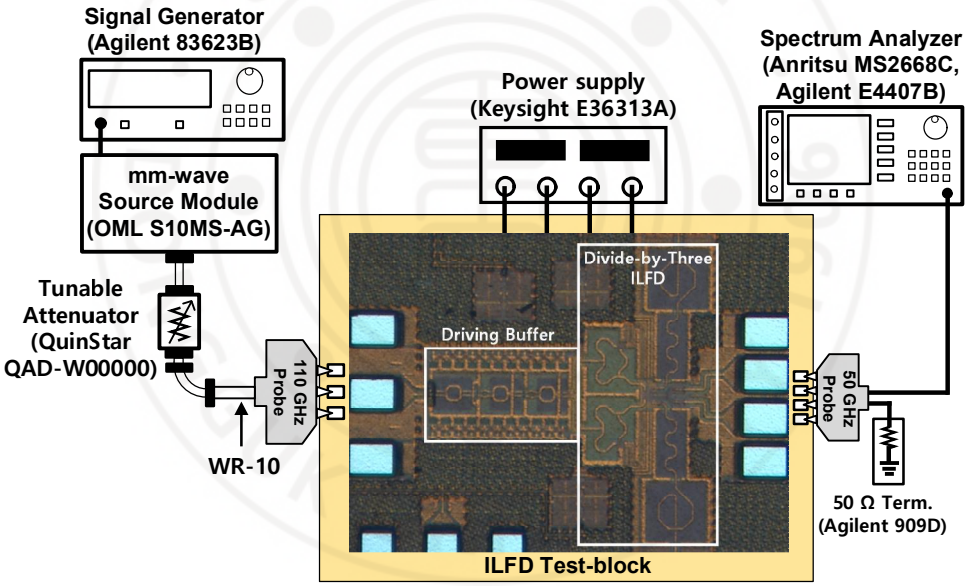


Figure VI-11. Measurement set-up for the proposed ILFD test-block with driving buffer.

6.3. Measurement results

The proposed divide-by-three ILFD was implemented with 65-nm CMOS process. Figure VI-10 shows a microphotograph of the chip (the core size is 0.68 × 0.33mm^2). The implemented ILFD consumed 7.88mA from a 1 V supply.

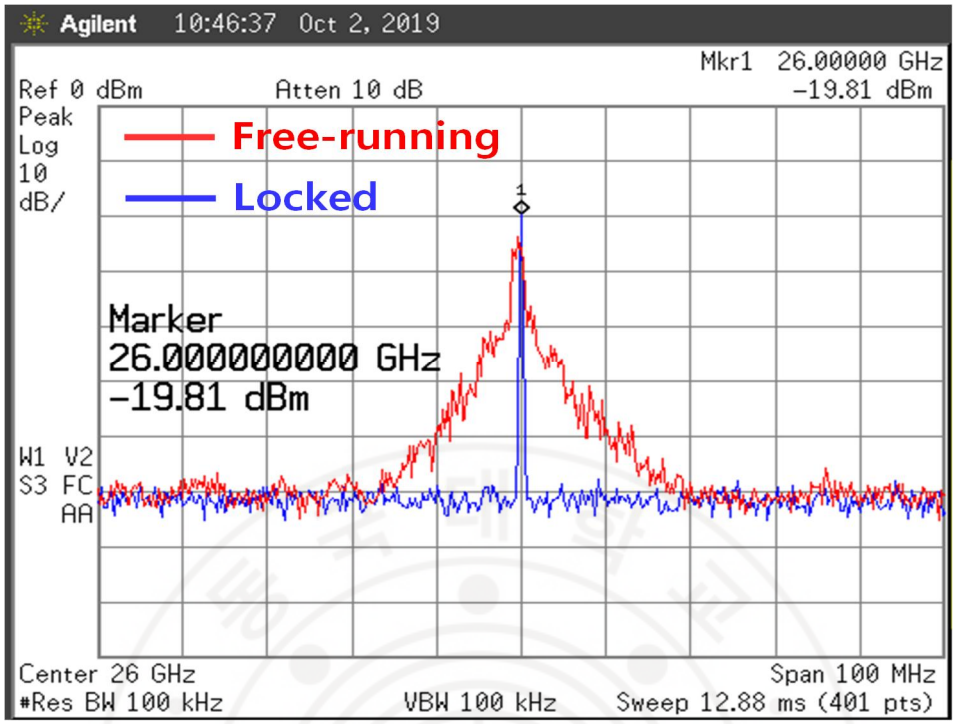


Figure VI-12. Measured spectra in free-running and locking state for the proposed ILFD with input frequency of 78GHz.

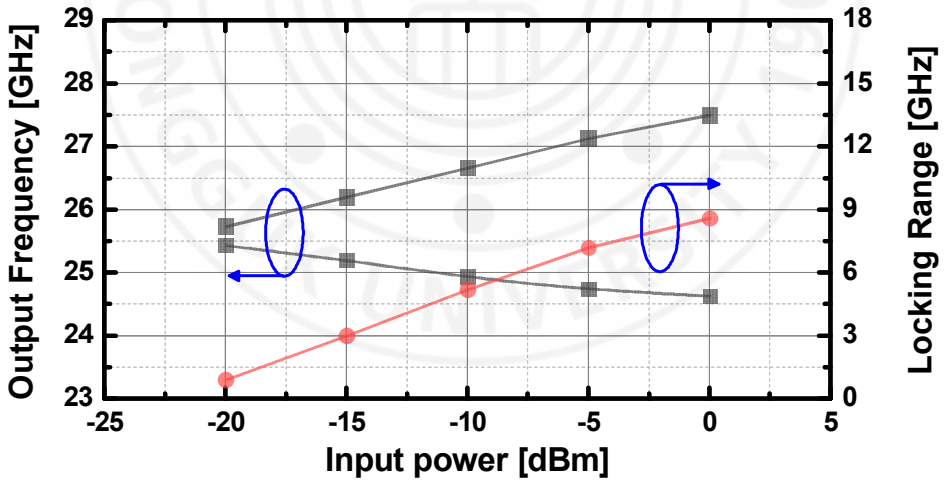


Figure VI-13. Measured sensitivity curve and locking range for the proposed ILFD.

As illustrated in Figure VI-11, Agilent 83623B signal generator with OML S10MS-AG mm-wave source module was used for a W-band input signal where Quinstar QAD-W00000 tunable attenuator was employed to control the input power level. Anritsu MS2668C/Agilent E4407B spectrum analyzers were used for the

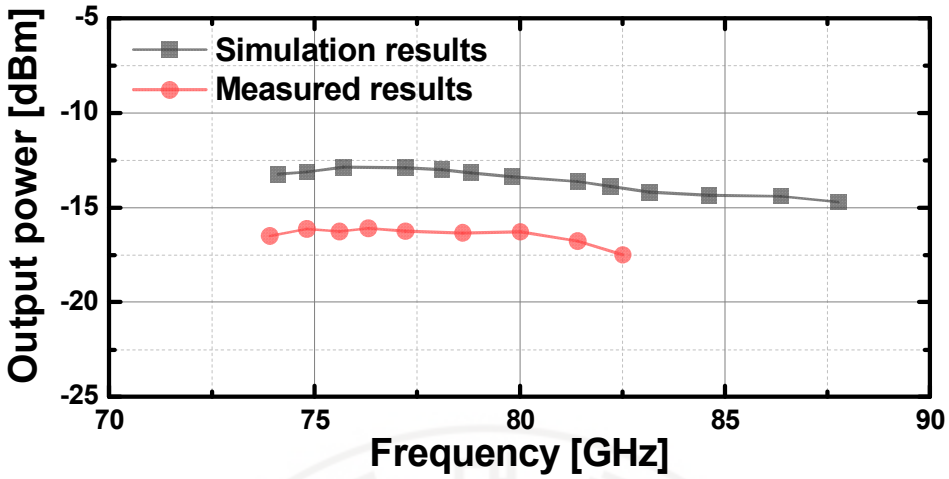


Figure VI-14. Simulated and measured output power for the proposed ILFD with input power of 0dBm. The measured output power is considered the loss caused by probe-tip and cable.

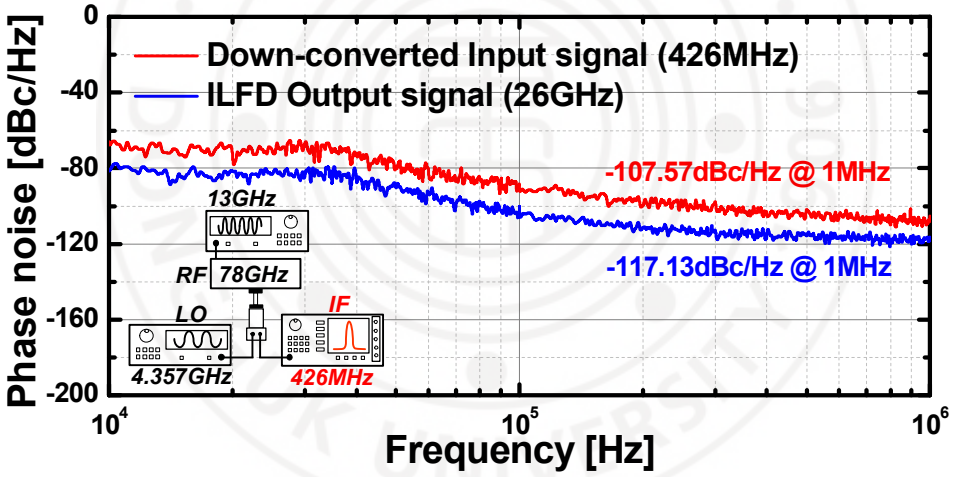


Figure VI-15. Measured phase noise for the proposed ILFD in locking condition. The phase noise of the input frequency was measured using by harmonic mixer (Agilent 11970W).

output spectrum and phase noise measurements. Since the output power from the W-band source module is lower than 0dBm considering the losses from the probe-tip and WR-10 wave guide, a characterized on-chip driving buffer with a power gain of 12dB was included in the test block.

Table VI-1. Comparison with previously reported mm-wave CMOS divide-by-three injection locked frequency dividers.

Ref.	**This work**	**[90]**	**[91]**	**[92]**	**[93]**	**[94]**	**[95]**	**[96]**
Tech.	65nm CMOS	130nm CMOS	130nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS
f_{max}. [GHz]	82.5	60	72.2	54.6	93.5	84.3	125.4	134.6
Locking Range	8.6GHz (10.9%)**	1.8GHz (3.1%)**	6.3GHz (9.12%)* 3.8GHz (5.5%)**	5.8GHz (11.2%)* 2GHz (3.8%)**	2.1GHz (2.3%)**	11.2GHz (14.2%)**	3GHz (2.4%)**	0.4GHz (0.29%)**
P_{in} [dBm]	0	0	7	2	0	3	-6	-8.5
P_{DC} [mW]	7.88	13	2	3	3.7	10.8	9.1	2.3
FoM1 [GHz2/ mW2]	90.04	8.3	27.37	22.97	53.07	43.81	164.6	165.7
FoM2 [%/mW 2]	4.19	0.7	1.62	2.4	1.84	1.98	3.18	2.7
PN @ 1MHz [dBc/Hz]	-117.13	-131.36	-120.85	-115	-124.1	-125.43	N/A	> -115
Area [mm^2]	0.22***	0.68	0.069***	0.09***	0.56	0.52	0.04***	0.46

Locking Range (%) = Locking Frequency Range / Center Frequency, * with varactor, ** without varactor, *** core size,

Figure VI-12 presents the measured output spectra of the ILFD with free-running and locking conditions. The output spectrum of the locking state shows the better phase noise than that of the free-running state. The measured sensitivity curve and locking range for the implemented ILFD are presented in Figure VI-13. The measured ILFD worked properly from 73.9GHz to 82.5GHz (Locking range=8.6GHz) with an input power of 0dBm. At the input power of 0dBm, the simulated and measured output power after calibrating the insertion-loss from the probe-tip and cable is shown in Figure VI-14. As shown in Figure VI-15, the measured phase noise at 1 MHz offset frequency is about –117.13dBc/Hz. The phase noise difference between the input and output at 1 MHz offset is well matched with the predicted value (20log103 = 9.54dB).

Table VI-1 compares the implemented ILFD with previously reported mm-wave ILFDs in CMOS [90]-[96]. The comparison table reports two different figure-of-merits (FOMs) defined as in [94, 97]:

$$FoM_1 = \frac{LR(GHz) \times f_{\max}(GHz)}{P_{in}(mW) \times P_{DC}(\mathrm{mW})} \tag{6-2}$$

$$FoM_2 = \frac{LR(GHz)}{f_{center}(\mathrm{GHz})} \times 100\% \times \frac{Division\ \ ratio}{P_{in}(mW) \times P_{DC}(\mathrm{mW})} \tag{6-3}$$

The designed ILFD measured a locking range over 10% without any extra power consumption or frequency tuning varactor in W-band. Thus, it achieved the highest FoM_2 among the recently reported CMOS ILFDs owing to the proposed inductive feedback network in boosting the injection current substantially.

VII. Conclusions and Future Work

7.1. Conclusions

In this dissertation, the designs for RF transceiver front-end are demonstrated for wireless communication and sensing applications.

In chapter 2, a 1-13 GHz 5-stage LNA was implemented in 65 nm CMOS. The proposed transformer-based LNA with 14.92 mW of the power consumption, the achieved 18.21 dB of the maximum gain, minimum noise figure (NF) of 5.28 dB, input-referred 1 dB compression point of -21.43 dBm, and the group delay variation of ±31 psec. The realized 5-stage UWB LNA with transformer-based inter-stage network consumes the core size of 0.52 mm^2.

In chapter 3, an I/Q up-conversion chain was presented in a 65-nm CMOS process. The QSG is combined with I/Q mixers with 25% duty-cycle I/Q signals. In order to improve OIP3 in the chain, a negative GM stage after the transconductance (GM) stage in the upconverter was employed. The designed mixer achieved 9.12dB of Tx gain and 14.45dBm of OIP3 with 46.9dB of IRR. The designed upconverter consumes the power consumption of 48.7mW, and occupy only 0.57mm^2 of chip area including pads (0.35mm^2 excluding pads).

In chapter 4, using four independent 36-Gb/s 2^7-1 PRBS generators, an integrated 2–18 GHz four-channel compressed sensing receiver (CSRX) with a 128.5 × sub-Nyquist acquisition, a 36-GHz Nyquist rate, and a 280-MHz spectrum bandwidth was realized in 0.13-μm SiGe BiCMOS Technology. Each CSRX channel consists of band-equalized full-swing LO driving circuitry, a double-balanced passive mixer, and a 2–18 GHz broadband distributed amplifier. The proposed CSRX architecture with LO equalization is generally applicable for the application of lightweight receivers for ultra-fast real-time tracking of spectrums in various sectors.

In chapter 5, a full X-band transmit/receive module (TRM) chip for phased-array antenna systems was realized in 65-nm CMOS technology. The implemented TRM chip includes a BDGA, a 6-bit attenuator, a 6-bit passive phase shifter. Especially, in order to expand the operating frequency range for phase shifter, a resonant

frequency misalignment technique was used. An SPDT interface as a duplexer was also combined with a wideband PA and LNA for bi-directional control of the half-duplex transceiver In comparison to recently published CMOS based phased-array chips, the measured results for the implemented TRM chip showed the highset OP_{1dB}, gain and widest operating frequency range. Furthermore, the TRM has distinct advantage of low-power dissipation with a comparable RF performance as compared with several recently reported SiGe transceivers and III-V TRM chipsets.

In chapter 6, a W-band divide-by-three injection locked frequency divider (ILFD) is realized in a 65-nm CMOS process. The ILFD with the inductive feedback could achieve three times improved locking range as the expense of area, but without tuning varactor or additional power consumption. With 7.88mW of the power dissipation, the proposed ILFD achieved the locking range from 73.9GHz to 82.5GHz, and -117.13dBc/Hz of phase noise at 1MHz, which demonstrated the highest FOMs when compared to recently reported W-band CMOS ILFDs.

7.2. Suggestions for Future work

다중 대역을 커버하며 광대역에서 동작하는 고성능 증폭기 구현을 위해, 2 장에서 제안한 transformer 기반 inter-stage 이외에 cross-coupled transformer 등 칩 소형화 및 증폭기 이득에 유리한 설계 연구를 제안한다.

5G 무선통신 상용화 서비스가 Global 하게 진행중이지만 여전히 서비스 품질 개선 등 많은 문제점을 지니고 있다. 이를 해결하기 위해서는 5G 망 구축 설비투자가 절실한 상황이지만 비용문제 등 제약이 많이 따른다. 따라서, 3 장에서 제안한 선형성 및 칩 소형화에 유리한 송신기용 Up-converter 설계를 활용하여 동 성능대비 가격경쟁면에서 유리한 송수신기 설계 연구를 제안한다.

광대역에 산재되어 있는 신호를 압축센싱하여 sub-Nyquist 주파수에서 샘플링이 가능한 압축센싱 수신기 하드웨어는, 4 장에서 제안한 RF 신호를 하향 주파수 변환하는 수신기 이외에, 원신호를 복원하기 위한 ADC 등 digital 신호처리부가 필요하므로 이를 통합 구현하는 연구를 제안한다.

무선통신 및 센싱용 MIMO system 에 필수적으로 사용되는 phased-array 용 송수신모듈은 다양한 어플리케이션에 적용 가능하므로, 5 장에서 제안한 X-대역 송수신 모듈 이외에 높은 주파수 (W-대역 이상)에서 동작하는 beam-former 구현에 대한 연구를 제안한다.

W-대역 혹은 sub-THz 대역에서 동작하는 차량용 FMCW 레이더 모듈, 6G 무선통신 등 다양한 어플리케이션에 적용 가능한 송수신기의 구현을 위해,

6 장에서 다룬 inductive feedback 기반의 W-대역 주파수 분배기 설계를 활용한 LO 신호원 설계 연구를 제안한다.

In addition to the transformer-based inter-stage proposed in Chapter 2, we may consider a design approach with a cross-coupled transformer which is advantageous for a size miniaturization and gain boosting in implementing a high-performance amplifier that covers multiple bands.

5G wireless communication service is in progress globally, but it still has many issues in improving service quality. In order to resolve this issue, investment in improving the 5G network facility is urgently needed. At the same time, there are many restrictions due to the hardware cost. Therefore, we propose a study on the design of a transceiver that is advantageous in price competitiveness by utilizing the proposed up-converter design approach for the low cost transmitters, which is advantageous for linearity and chip miniaturization as proposed in Chapter 3.

Compressed sensing receiver capable of compressing and sensing the signals scattered in the wideband at sub-Nyquist frequency necessitates an interface circuitry such as ADC in restoring the original signal. The interface circuit should be co-designed and optimized with the compressed sensing receiver in Chapter 4.

Since the phased-array transmit/receive module (TRM) is essential to the MIMO system for wireless communication and sensing, and it is applicable to various applications, it is quite important topic to implement an efficient TRM operating at a high frequency (W-band or higher) in addition to the X-band TRM suggested in Chapter 5.

In order to implement a transceiver for various applications such as FMCW radar modules for vehicles in the W-band or 6G wireless communication in sub-THz band, a LO signal generator can be fully integrated in CMOS by employing the inductive feedback-based W-band frequency divider design described in Chapter 6.

REFERENCES

[1] H. T. Friis, “A Note on a Simple Transmission Formula,” Proc. IRE, vol. 34, no. 5, pp. 254–256, 1946.

[2] R. Emrick, S. Franson, J. Holmes, B. Bosco, and S. Rockwell, “Technology for emerging commercial applications at millimeter-wave frequencies,” in IEEE/ACES International Conference on, April 2005, pp. 425-429.

[3] J. Powell and D. Bannister, “Business prospects for commercial mm-wave MMICs,” IEEE Microwave Magazine, vol. 6, no. 4, pp. 34-43, Dec. 2005.

[4] G. E. Moore, “Cramming more components onto integrated circuits,” Proceeding of the IEEE, vol. 86 , no. 1, pp. 82-85 , Jan. 1998.

[5] (2020) ISSCC Press Kit, [Online]. Available: http://isscc.org/

[6] C.-H. Jan, M. Agostinelli, H. Deshpande, M.A. El-Tanani, W. Hafez, U. Jalan, L. Janbay, M. Kang, H. Lakdawala, J. Lin, Y.-L. Lu, S. Mudanai, J. Park, A. Rahman, J. Rizk, W.-K. Shin, K. Soumyanath, H. Tashiro, C. Tsai, P. Van-DerVoorn, J.-Y. Yeh, and P. Bai, “RF CMOS technology scaling in high-k/metal gate era for RF soc (system-on-chip) applications,” in 2010 IEEE International Electron Devices Meeting (IEDM), pp. 27.2.1-27.2.4, Dec. 2010.

[7] R. Lombardi, “Microwave and Millimetre-wave for 5G Transport,” ETSI White Paper, no. 25, [Online]. Available: https://www.etsi.org/

[8] F. Boccardi, R. Heath, A. Lozano, T. L. Marzetta, and P. Popovski, “Five disruptive technology directions for 5G,” IEEE Commun. Mag., vol. 52, no. 2, pp. 74–80, 2014.

[9] A. Gupta and R. K. Jha, “A Survey of 5G Network: Architecture and Emerging Technologies,” IEEE Access, vol. 3, pp. 1206–1232, 2015.

[10] T. S. Rappaport et al., “Millimeter wave mobile communications for 5G cellular: It will work!,” IEEE Access, vol. 1, pp. 335–349, 2013.

[11] J. G. Andrews et al., “What will 5G be?,” IEEE J. Sel. Areas Commun., vol. 32, no. 6, pp. 1065–1082, 2014.

[12] LAN/MAN Standards Committee, Part 11 : Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications Amendment 3 : Enhancements for Very High Throughput in the 60 GHz Band, vol. 2012, no. December. 2012.

[13] M. Boers et al., “A 16TX/16RX 60 GHz 802.11ad chipset with single coaxial interface and polarization diversity,” IEEE J. Solid-State Circuits, vol. 49, no. 12, pp. 3031–3045, 2014.

[14] P. Daponte et al., “Analog-to-information converters in the wideband RF measurement for aerospace applications: current situation and perspectives,” IEEE Inst. Meas. Mag., vol. 20, no. 1, pp. 20–28, Feb. 2017.

[15] V. H. C. Chen and L. Pileggi, “A 69.5 mW 20 GS/s 6b time-interleaved ADC with embedded time-to-digital calibration in 32 nm CMOS SOI,” in ISSCC Dig. Tech. Papers, pp. 380–381, 2014.

[16] "High-performance digitizers for advanced scientific research" Agilent [Online]. Available: http://cp.literature.agilent.com/

[17] A. Hajimiri, et. al., “Phased array system in silicon,” IEEE Commun. Mag., vol. 42, no. 8, Aug. 2004, pp. 122-130.

[18] A. Lozano, et. al. “Lifting the limits on high-speed wireless data access using antenna arrays,” IEEE Commun. Mag., vol. 39, no. 9, Sept. 2001, pp. 156-162.

[19] R. G. Vaughan and J. B. Andersen, “Antenna diversity in mobile communications,” IEEE Trans. Vehic. Tech., vol. 36, no. 4, Nov. 1987, pp. 149-72.

[20] S. M. Alamouti, “A simple transmit diversity technique for wireless communications,” IEEE JSAC, vol. 16, no. 8, Oct. 1998, pp. 1451-58.

[21] R. D. Murch and K. B. Letaief, “Antenna systems for broadband wireless access,” IEEE Commun. Mag., vol. 40, no. 4, Apr. 2002, pp. 76-83

[22] C. H. Doan, et. al., “Design considerations for 60GHz CMOS radios,” IEEE Commun. Mag., vol. 42, no. 12, Dec. 2004, pp. 132-140.

[23] A. Ismail and A. A. Abidi, “A 3–10 GHz low noise amplifier with wideband LC-ladder matching network,” IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2269–2277, Dec. 2004.

[24] A. Bevilacqua and A. M. Niknejad, “An ultrawideband CMOS low noise amplifier for 3.1–10.6 GHz wireless receivers,” IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.

[25] X. Fan, E. Sánchez-Sinencio, and J. Silva-Martinez, “A 3 GHz–10 GHz common gate ultrawideband low noise amplifier,” in Proc. IEEE Midwest Symp. Circuits and Systems, Aug. 2005, pp. 631–634.

[26] K. Chen, J. Lu, B. Chen, and S. Liu, “An ultra-wide-band 0.4–10 GHz LNA in 0.18-μm CMOS,” IEEE Trans. Circuits Syst. II, Express Briefs, vol. 54, no. 3, pp. 217–221, Mar. 2007.

[27] C. F. Liao and S. I. Liu, “A broadband noise-canceling MOS LNA for 3.1–10.6-GHz UWB receiver,” IEEE J. Solid-State Circuits, vol. 42, no. 2, pp. 329–339, Feb. 2007.

[28] W. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, “A highly linear broadband CMOS LNA employing noise and distortion cancellation,” IEEE J. Solid-State Circuits, vol. 43, no. 5, pp. 1164–1176, May 2008.

[29] S. Shekhar, J. S.Walling, and D. J. Allstot, “Bandwidth extension techniques for CMOS amplifiers,” IEEE J. Solid-State Circuits, vol. 41, no. 11, pp. 2424–2438, Nov. 2006.

[30] H. Nam, and J.-D. Park, “A 1-13 GHz CMOS Low-Noise Amplifier using Compact Transformer-based Inter-stage Networks,” IEICE Electronics Express 15 (2018) 20171019.

[31] J. –D. Jin and S. S. H. Hsu, “A 40-Gb/s transimpedance amplifier in 0.18-μm CMOS Technology,” IEEE J. Solid-State Circuits, vol. 43, no. 6, pp. 1449–1457, Jun. 2008.

[32] Y. –S. Lin, C. –Z, Chen, H. –Y. Yang, C. –C. Chen, J. –H. Lee, G. –W. Huang, and S. –S. Lu, “Analysis and design of a CMOS UWB LNA with the dual-RLC branch wideband input matching network,” IEEE Trans. Microw. Theory Tech., vol. 58, no. 2, pp. 287–296, Feb. 2010.

[33] Q. Li and Y. P. Zhang, “A 1.5-V 2–9.6-GHz inductorless low-noise amplifier in 0.13-μm CMOS,” IEEE Trans. Microw. Theory Tech., vol. 55, no. 10, pp. 2015–2023, Oct. 2007.

[34] D. Pepe and D. Zito, “22.7-dB Gain −19.7-dBm ICP1dB UWB CMOS LNA,” IEEE Trans. Circuits Syst. II, Express Briefs, vol. 56, no. 9, pp. 689–693, Sep. 2009.

[35] Y. –S. Lin, C. –C. Wang, G. –L. Lee, and C. –C. Chen, “High-performance wideband low-noise amplifier using enhanced π-match input network,” IEEE Microw. Compon. Lett., vol. 24, no. 3, pp. 200–202, Mar. 2014.

[36] J. W. Roh et al., “Millimeter-wave beamforming as an enabling technology for 5G cellular communications: Theoretical feasibility and prototype results,” IEEE Comm.Mag., vol. 52, pp.106–113, Feb. 2014.

[37] Y. Cho et al., “A 16-element phased-array CMOS transmitter with variable gain controlled linear power amplifier for 5G new radio,” in Proc. IEEE Radio Freq. Integr. Circuits Symp., Jun. 2019, pp. 247–250.

[38] J.-G. Lee et al., “60 GHz direct up-conversion mixer with wide IF bandwidth and high linearity in 65 nm CMOS,” in Proc. IEEE RFIT, Seoul, South Korea, 30 Aug.-1 Sept. 2017, pp. 74–76.

[39] C. W. Byeon et al., “A high linearity, image/LO-rejection I/Q up-conversion mixer for 5G cellular communications,” in Proc. EuMC, Paris, France, Sep. 2015, pp. 345–348.

[40] Y.-S. Won et al., “A 24 GHz highly linear up-conversion mixer in CMOS 0.13 μm technology,” IEEE Microw. Compon. Lett., vol. 25, no. 6, pp. 400–402, Jun. 2015.

[41] D. Im et al., “A wideband CMOS low noise amplifier employing noise and IM2 distortion cancellation for a digital TV tuner,” IEEE J. Solid-State Circuits, vol. 44, No. 3, pp. 686-698, Mar. 2009.

[42] H. Nam, W. Lee, J. H. Son, and J.-D. Park, “A Compact I/Q Up-Conversion Chain for a 5G Wireless Transmitter in 65-nm CMOS Technology,” IEEE Microw. Wireless Compon. Letters, vol.30, no.3, March 2020, pp.284-287.

[43] S. Lou et al., “A linearization technique for RF receiver front-end using second-order-intermodulation injection” IEEE J. Solid-State Circuits, vol. 43, no. 11, pp.2404-2412, Nov. 2008.

[44] W. Cheng et al., “A flicker noise/IM3 cancellation technique for active mixer using negative impedance,” IEEE J. Solid-State Circuits, vol. 48, no. 10, pp. 2390–2402, Oct. 2013.

[45] S. Zhou et al., “A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver,” IEEE J. Solid-State Circuits, vol. 40, no. 5, pp. 1084–1093, May 2005.

[46] D. Kaczman *et al.*, “A single-chip 10 Band WCDMA/HSDPA 4-band GSM/EDGE SAW-less CMOS receiver with DigRF 3G interface and +90dBm IIP2,” *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 718–739, Mar. 2009.

[47] Y.-J. Ko *et al*., “Gain and phase mismatch effects on double image rejection transmitter,” *IET Circuits Devices Syst.,* vol. 5, no. 3, pp. 212–221, May 2011.

[48] J. Yoo et al., “A compressed sensing parameter extraction platform for radar pulse signal acquisition,” IEEE J. Emerg. Sel. Topics Circuits Syst., vol. 2, no. 3, pp. 626–638, Sep. 2012.

[49] R.T. Yazicigil et al., “Wideband rapid interferer detector exploiting compressed sampling with a quadrature analog-to-information converter,” IEEE J. Solid-State Circuits, vol. 50, no. 12, pp. 3047–3064, Dec. 2015.

[50] J. Yoo et al., “A 100 MHz-2 GHz 12.5×sub-Nyquist rate receiver in 90 nm CMOS,” in Proc. IEEE RFIC Conf., pp. 31–34. 2012.

[51] M. Mishali and Y. C. Eldar, “From theory to practice: sub-Nyquist sampling of sparse wideband analog signals,” IEEE J. Sel. Top. Signal Process., vol. 4, no. 2, pp. 375–391, Apr. 2010.

[52] D. L. Donoho, “Compressed sensing,” IEEE Trans. Inf. Theory, vol. 52, no. 4, pp. 1289–1306, Apr. 2006.

[53] E. J. Candès and M. Wakin, “An introduction to compressive sampling,” IEEE Signal Process. Mag, vol. 25, no. 2, pp. 21–30, Feb. 2008.

[54] H. Nam, J. Park, J.-D. Park, “A 2–18 GHz Compressed Sensing Receiver with Broadband LO chain in 0.13-μm SiGe BiCMOS," IEEE Microw. Wireless Compon. Letters, vol. 29, no. 9, pp. 620–622, March 2019.

[55] J. N. Laska et al., “Theory and implementation of an analog-to-information converter using random demodulation,” in Proc. IEEE Int. Symp. Circuits Syst., pp. 1959–1962, 2007.

[56] F. Sinnesbichler et al., “Generation of high-speed pseudorandom sequences using multiplex-techniques,” IEEE Trans. Microw. Theory Tech., vol. 44, no. 12, pp. 2738–2742, Dec., 1996.

[57] A. Gharib et al., “A broadband 1.35THz GBP 120-mW common-collector feedback amplifier in SiGe technology,” in IEEE Bipolar/BiCMOS Circ. Tech. Meeting (BCTM), pp. 72–75, Oct. 2012.

[58] A. de Boer and K. Mouthaan, “GaAs mixed signal multi-function X-band MMIC with 7 bit phase and amplitude control and integrated serial to parallel converter,” in Proc. Eur. Microw. Conf., Oct. 2000, pp. 1–4.

[59] D M. van Heijninggen et al., ″Multi function and high power amplifier chipset for X-band phased array frontends,″in Proc. 1st Eur. Microw. Int. Cir. Conf., Sep. 2006, pp. 237–240.

[60] J. Jeong and I. Yom, ″X-band high power SiGe BiCMOS multi-function chip for active phased array radars,″Electron. Lett., vol. 47, no. 10, pp. 618–619, Dec. 2011.

[61] D. Carosi, A. Bettidi, A. Nanni, L. Marescialli, and A. Cetronio, ″A mixed-signal X-band SiGe multi-function control MMIC for phased array radar applications,″in Proc. 39th Eur.Microw. Conf., Oct. 2009, pp. 240–243.

[62] K.-J. Koh and Rebeiz, ″An X- and Ku-band 8-element phased-array receiver in 0.18 μm SiGe BiCMOS technology,″IEEE J. Solid-State Circuits, vol. 43, no. 6, pp. 1360–1371, Jun. 2008.

[63] J. P. Comeau, M. A. Morton, W.-M. L. Kuo, T. Thrivikraman, J. M. Andrews, C. M. Grens, J. D. Cressler, J. Papapolymerou, and M. Mitchell, ″A silicon–germanium receiver for X-band transmit/ receive radar modules,″ IEEE J. Solid-State Circuits, vol. 43, no. 9, pp. 1889–1896, Sep. 2008.

[64] C. Liu, Q. Li, Y. Li, X.-D. Deng, X. Li, H. Liu, and Y.-Z. Xiong, “A fully integrated X-band phased-array transceiver in 0.13-μm SiGe BiCMOS technology,” IEEE Trans. Microw. Theory Techn., vol. 64, no. 2, pp. 575–584, Feb. 2016.

[65] P. Lohmiller, R. Reber, P. Schuh, M. Oppermann, and S. Chartier, “SiGe BiCMOS X-band transceiver-chip for phased-array systems,” in Proc. 47th Eur.Microw. Conf., Oct. 2017, pp. 1253–1256.

[66] P. Saha, S. Muralidharan, J. Cao, O. Gurbuz, and C. Hay, "X/Ku-band four-channel transmit/receive SiGe phased-array IC", in 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC),, pp. 51-54, 2019.

[67] Z. Hao and W. Chuanchuan, "A 8-12GHz 4-element SiGe BiCMOS multi-function chip for phased array systems," in 2019 IEEE Integrated Circuits and Microsystems (ICICM), pp. 95-99, 2019.

[68] D. Shin and G. Rebeiz, ″A high-linearity X-band four-element phased-array receiver: CMOS chip and packaging,″ IEEE Trans. Microw. Theory Techn., vol. 59, no. 8, pp. 2064–2072, Aug. 2011.

[69] K. Gharibdoust, N. Mousavi, M. Kalantari, M. Moezzi, and A. Medi, ″A fully integrated 0.18-μm CMOS transceiver chip for X-band phased-array systems,″ IEEE Trans. Microw. Theory Techn., vol. 60, no. 7, pp. 2192–2202, Jul. 2012.

[70] S. Sim, L. Jeon, and J.-G. Kim, ″A compact X-band bi-directional phased-array T/R chipset in 0.13 μm CMOS technology,″IEEE Trans. Microw. Theory Techn., vol. 61, no. 1, pp. 562–569, Jan. 2013.

[71] D. Shin, C.-Y. Kim, D.-W. Kang, and G. M. Rebeiz, ″A high-power packaged four-element X-band phased-array transmitter in 0.13-μm CMOS for radar and communication systems,″IEEE Trans. Microw. Theory Techn., vol. 61, no. 8, pp. 3060–3071, Aug. 2013.

[72] V.-V. Ngyuen, H. Nam, Y. J. Choe, B.-H. Lee and J.-D. Park, “An X-band bi-directional transmit/receive module for a phased array system in 65-nm CMOS,” Sensors, vol. 18, no. 8, p. 2569, 2018.

[73] S. Sim, B. Kang, J.-G. Kim, J.-H. Chun, B. Jang, and L. Jeon, “A four-channel bi-directional CMOS core chip for X-band phased array T/R modules,” in Proc. IEEE Radar Conf. (RadarCon), May 2015, pp. 1198–1201.

[74] K. Koh and G. M. Rebeiz, "0.13-μm CMOS phase shifters for X-, Ku-, and K-band phased arrays," IEEE J. Solid-State Circuits, vol. 42, no. 11, pp. 2535-2546, Nov. 2007.

[75] M. A. Morton, J. P. Comeau, J. D. Cressler, M. Mitchell and J. Papapolymerou, "Sources of phase error and design considerations for silicon-based monolithic high-pass/low-pass microwave phase shifters," IEEE Trans. Microw. Theory Tech., vol. 54, no. 12, pp. 4032-4040, Dec. 2006.

[76] B. Min and G. M. Rebeiz, "Single-ended and differential Ka-band BiCMOS phased array front-ends," IEEE J. Solid-State Circuits, vol. 43, no. 10, pp. 2239-2250, Oct. 2008.

[77] H. Nam, V.-V. Nguyen, V.-S. Trinh, J.-M. Song, B.-H. Lee and J.-D. Park, “A Full X-band Phased-Array Transmit/Receive Module Chip in 65-nm CMOS Technology,” IEEE Access, vol. 8, 2020, pp.76182-76192.

[78] V.-V. Nguyen, “An X-Band Bi-Directional Transmit/Receive Module for a Phased Array System in 65-nm,” M.S. thesis, Dongguk University, Seoul, Republic of Korea, 2019.

[79] R. V. Garver, “Broad-band diode phase shifters,” IEEE Trans. Microw. Theory Tech., vol. MTT-20, no. 5, pp. 314-323, May 1972.D

[80] F. Zhang and P. R. Kinget, “Low-power programmable gain CMOS distributed LNA,” IEEE J. Solid-State Circuits, vol. 41, no. 6, pp. 1333–1343, Jun. 2006.

[81] J. Chen and A. M. Niknejad, “Design and analysis of a stage-scaled distributed power amplifier,” IEEE Trans. Microw. Theory Techn., vol. 59, no. 5, pp. 1274–1283, May 2011.

[82] V.-S. Trinh, H. Nam, and J.-D. Park, “A 20.5-dBm X-band power amplifier with a 1.2-V supply in 65-nm CMOS technology,” IEEE Microw. Wireless Compon. Lett., vol. 29, no. 3, pp. 234–236, Mar. 2019.

[83] H. Wang, C. Sideris, and A. Hajimiri, “A CMOS broadband power amplifier with a transformer-based high-order output matching network,” IEEE J. Solid-State Circuits, vol. 45, no. 12, pp. 2709–2722, Dec. 2010.

[84] S. P., J. Jeong, C. D. Presti, A. Scuderi, and P. M. Asbeck, “A watt-level stacked-FET linear power amplifier in Silicon-on-Insulator CMOS,” IEEE Trans. Microw. Theory Techn., vol. 58, no. 1, pp. 57–64, Jan. 2010.

[85] B.-H. Ku, S.-H. Baek, and S. Hong, “A wideband transformer-coupled CMOS power amplifier for X-band multifunction chips,” IEEE Trans.Microw. Theory Techn., vol. 59, pp. 1599–1609, June 2011.

[86] J.-O. Plouchart, J. Kim, V. Karam, R. Trzcinski, and J. Gross, “Performance variations of a 66 GHz static CML divider in 90 nm CMOS,” in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2006, pp. 2142–2151.

[87] D. Lim, J. Kim, J.-O. Plouchart, C. Cho, D. Kim, R. Trzcinski, and D. Boning, “Performance variability of a 90 GHz static CML frequency divider in 65 nm SOI CMOS,” in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2007, pp. 542–543.

[88] A. Ghilioni, A. Mazzanti, and F.Svelto, "Analysis and design of mm-wave frequency dividers based on dynamic latches with load modulation," IEEE J. Solid-State Circuits, vo1.48, no 8, Aug. 2013, pp. 1842-1850.

[89] B. Razavi, “A study of injection locking and pulling in oscillators,” IEEE J. Solid-State Circuits, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[90] H. Wu and L. Zhang, “A 16-to-18 GHz 0.18 μm Epi-CMOS divide-by-3 injection locked frequency divider,” in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2006, pp. 602–603.

[91] T.-N. Luo, S.-Y. Bai, and Y.-J. E. Chen, “A 60-GHz 0.13-μm CMOS divide-by-three frequency divider,” IEEE Trans. Microw. Theory Tech., vol. 56, no. 11, pp. 2409–2415, Nov. 2008.

[92] C.-H. Wang et al., “A 66-72 GHz divide-by-3 injection locked frequency divider in 0.13- m CMOS technology,” in Proc. IEEE Asian Solid-State Circuits Conf., Nov. 2007, pp. 344–347.

[93] X. P. Yu, H. M. Cheema, R. Mahmoudi, A. van Roermund, and X. L. Yan, “A 3 mW 54.6 GHz divide-by-3 injection locked frequency divider with resistive

harmonic enhancement," IEEE Microw. Wireless Compon. Lett., vol. 19, no. 9, pp. 575–577, Sep. 2009.

[94] Y.-L. Yeh and H.-Y. Chang, "Design and analysis of a -band divide-by-3 injection locked frequency divider using second harmonic enhancement technique," IEEE Trans. Microw. Theory Techn., vol. 60, no. 6, pp. 1617–1625, Jun. 2012.

[95] Y.-W. Chen, T.-N. Luo, H. Cruz, and Y.-J. E. Chen, "A W-Band harmonically enhanced CMOS divide-by-three frequency divider," IEEE Microw. Wireless Compon. Lett., vol. 24, no. 4, pp. 257–259, Apr. 2014.

[96] I.-T. Lee, C.-H. Wang, J.-R. Sha, Y.-Z. Juang and S.-I. Liu, "D-band divide-by-3 injection-locked frequency divider in 65 nm CMOS," Electron. Lett., vol. 48, no. 17, pp. 1041-1042, Aug. 2012.

[97] Y.-L. Yeh, Y.-C Liu, H.-Y. Chang, and K. Chen, "Evaluation of a D-band divide-by-3 injection-locked frequency divider in 65 nm CMOS process," in Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol. (RFIT), May 2015, pp. 184–186.

[98] Y.-H. Kuo, J.-H. Tsai, H.-Y. Chang, and T.-W. Huang, "Design and analysis of a 77.3% locking-range divide-by-4 frequency divider," IEEE Trans. Microw. Theory Tech., vol. 59, no. 10, pp. 2477–2485, Oct. 2011.

[99] K. T. Yamamoto, T. Norimatsu, and M. Fujishima, "1 V 2 GHz CMOS frequency divider," Electron. Lett., vol. 39, no. 17, pp. 1227–1228, Aug. 2003.

[100] J. H. Cheng, J. H. Tsai and T. W. Huang, "Design of a 90.9% locking range injection-locked frequency divider with device ratio optimization in 90-nm CMOS," IEEE Trans. Microw. Theory Tech., vol. 65, no.1, pp.187-197, Jan. 2017.

[101] J.-C. Chien and L.-H. Lu, "Analysis and design of wideband injectionlocked ring oscillators with multiple-input injection," IEEE J. Solid State Circuits, vol. 42, no. 9, pp. 1906–1915, Sep. 2007.

[102] H. Nam, and J.-D. Park, "A W-band Divide-by-Three Injection Locked Frequency Divider with Injection Current Boosting Utilizing Inductive Feedback in 65nm CMOS," IEEE Microw. Wireless Compon. Letters, vol.30, no.5, May 2020, pp.516-519.