Thesis for the Degree of Master of Engineering

Design of High-Power Low Insertion Loss Transmit/Receive (TR) Switch and Robust High Gain Low Noise Amplifier (LNA) in 250nm GaN Technology

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by

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Finally, I would like to thank my family for everything.

ABSTRACT

This thesis presents an X-band low noise amplifier (LNA) and a single-pole double-through (SPDT) transmit/receive switch which constructs a receive channel in active electronically scanned array (AESA) radars. The chips are designed based on high bandgap material Gallium Nitride (GaN). By utilizing λ/4 transmission lines and shunt transistors without series transistors, the T/R switch can endure a tremendous amount of power level and shows a good insertion loss with high isolation as well. The SPDT switch covers the whole X band with return loss is better than 10dB, insertion loss is smaller than 1.35dB while achieving isolation of 35dB in simulation. The large-signal simulation shows that the switch can handle 41dBm continuous incident waves in 1dB degradation. Meanwhile, a 4-stages conventional LNA was designed for the block placed next to the SPDT T/R switch in the receive path. The proposed LNA achieved a minimum noise figure (NF) of 2.1 dB at 10 GHz with less than 2.8dB within the operating bandwidth, a small signal power gain of 30 dB while maintaining the output power less than 25dBm to protect the block next to the LNA.

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I. Introduction

1.1. Motivation

Nowadays, the AESA is growing rapidly with applications in military and commercials as well. AESA systems are based on the working principle of normal radars, in which a transmitter (Tx) sends a short signal pulse through an antenna. Using a switch, the antenna is then disconnected from Tx and connected to an Rx. A delay time of the returned signal can be used to determine the distance to the reflecting object. AESA systems send a signal from a single source (called the main station) to an array of TRx modules, each of which can control the phase of the signal independently (Figure 1.1). AESA radar can scan the space much faster than mechanical systems because the beam can be steered quickly this way. Additionally, since AESA radar is capable of producing sub-beams at different frequencies, it can track a large number of targets simultaneously.

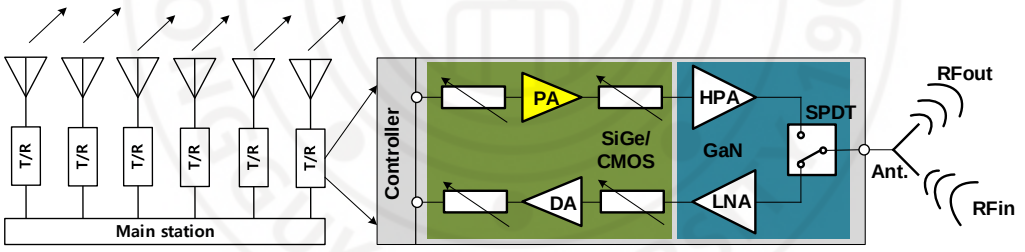

Figure 1. 1 Simplified block diagram of AESA system.

Also shown in Fig 1.1 is a block diagram of current AESA T/R modules (TRM). TRMs are usually composed of a front-end module that is connected to the antenna and a back-end module that is connected to the main station. The front-end block is typically implemented on GaN technologies. Due to the very high g_m of these technologies, we could design very high-power power amplifiers (PAs) (in the range of 46 dBm [1]). A

GaN LNA and switch can also achieve very good performance. However, GaN technologies have the disadvantage of being difficult to integrate. Therefore, the back-end module with phase controllability is typically designed in SiGe or CMOS processes. To compensate for the loss of the passive phase delay blocks, it still requires a driving amplifier and power amplifiers in the back-end module, which is normally required to provide up to >20-dBm output power at the transmitting path to sufficiently drive the front-end HPA.

In this dissertation, a low insertion, high-power handling capability SPDT switch and a low noise figure, high gain LNA are presented. These chips are fabricated in 0.25μm GaN and measured to check the accuracy of simulation results. From the measurements results, the switch achieved 1.3dB insertion loss and 35dB isolation at X band. Besides, under the large signal measurement, it can handle 41dBm input power level within 1dB degradation. While LNA shows a NF of 2.1dB, and a small signal gain of 30dB at 10GHz.

1.2. GaN Technology – The pros and cons

RF/microwave systems that need high power handling capabilities and low noise figures are getting a lot more attention to GaN technology. GaN electronics have been given a boost since then, and today the technology improves the performance of various applications including mobile communication, communication, and military radar systems, it is focusing on further advantages such as energy efficiency and reducing the global impact of energy consumption.

Monolithic MMIC-based semiconductor technologies have in the past achieved significant performance improvements in terms of being able to handle high levels of power, higher gains, higher efficiency, and lower noise levels.

GaN was shown to be an ideal solution for combining high frequency and power requirements in the early 1990s. A GaN material is capable of meeting system requirements from low frequencies [2],[3] to millimeter waves [4]-[6] and has been recognized as a very useful material for high power applications. Due to GaN technology's special properties, it truly qualifies as a disruptive wide band gap technology that affords a much higher level of energy than other technologies, for instance gallium arsenide (GaAs), indium phosphide (InP), and silicon (Si). Consequently, current densities over 2 A/mm have been reported [13-14]. Using field-plated devices, Cree has reported high power densities of 40 W/mm at 4 GHz with 1.2 A/mm. HRL, Raytheon, and Fujitsu have demonstrated and reported watt-level output power in the W-band in [4]-[6]. For current gain frequencies, Ft, greater than 40 GHz, Cree demonstrated power densities of more than 25 W/mm of gate periphery in [7]. Figure II.1 summarizes the most commonly used semiconductor technologies and their limitations in terms of power handling capabilities and operating frequencies.

GaN is characterized by a high breakdown field, a high electron mobility, and a very high saturation velocity. As a result of GaN's excellent thermal conductivity and the fact that it can operate at high temperatures, it is an ideal material for high-power and high-temperature microwave applications. Further, GaN has the potential to enable next-generation wireless and satellite communication systems with high-speed data transmission, power-efficient wireless systems, reduced carbon footprints for wireless networks, and interoperability across diverse communication standards. HEMTs and HFETs made of gallium nitride are currently the most advanced nitride based devices. The undoped GaN heterostructure has many advantages, including high breakdown and transport properties.

Table 1.1 compares the physical and electrical properties of widely used semiconductor technologies. GaN provides high power output due to its high sheet carrier density and channel charge density. Moreover, it has a high electron mobility, contributing to high power added efficiency at high frequencies, as well as low resistance. Thus, GaN HEMTs are capable of achieving much higher breakdown voltages than other technologies, as well as very high current densities and high channel operating temperatures. TriQuint's GaAs 0.25μm process has a breakdown voltage of approximately 15V [9], while its GaN 0.25μm process has a breakdown voltage of approximately 100V [10]. Additionally, active devices can operate at high speeds due to a combination of high electron mobility and saturation velocity. GaN circuits have been demonstrated to operate at high frequencies while maintaining acceptable efficiency.

Table 1. 1. Comparison between properties of the most commonly used semiconductor technologies [8]

	Si	GaAs	4H-SiC	GaN	Diamond
E_g	1.1	1.42	3.26	3.39	5.45
$n_i\ (cm^{-3})$	$1.5\text{x}10^{10}$	$1.5\text{x}10^{6}$	$8.2\text{x}10^{-9}$	$1.9\text{x}10^{-10}$	$1.6\text{x}10^{-27}$
ε_r	11.8	13.1	10	9.0	5.5
$\mu_n\ (cm^2/Vs)$	1350	8500	700	1200(Bulk) 2000 (2DED)	1900
$v_{sat}(10^7 cm/s)$	1.0	1.0	2.0	2.5	2.7
$E_{br}(MV/cm)$	0.3	0.4	3.0	3.3	5.6
$\Theta\ (W/cm\ K)$	1.5	0.43	3.3-4.5	1.3	20
$JM = \frac{E_{br} v_{sat}}{2\pi}$	1	2.7	20	27.5	50

GaN devices are indirectly more efficient because of all of these factors. A second advantage of this device is its ability to grow epitaxially on SiC substrates, which have excellent thermal properties.

Despite GaN's superior characteristics, numerous fabrication issues (process, device, circuit, and system) still need to be addressed before it can be widely adopted. Technical (device processing) and commercial challenges affect the development of GaN technology.

In Figure 1.2, two important effects are shown that cause current dispersion on GaN HEMTs: the trapping effect and thermal effect. Due to the dispersion present in GaN devices, the drain current and voltage excursions are restricted, which limits the device's performance in high power and high frequency applications.

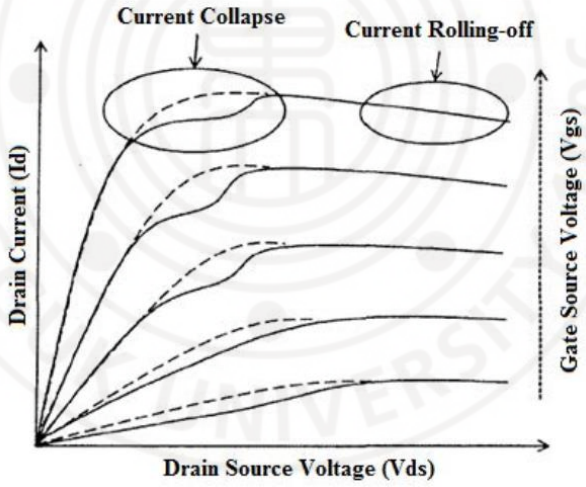

Figure 1. 2 Current due to trapping effect and thermal effect [11]

Trapping effects result in a temporary reduction in drain current response called current collapse. According to this theory, some electrons are trapped within AlGaN/GaN HEMT heterostructures [11], as shown in Figure 1.3. Electrons trapped in the channel reduce sheet electron density, increasing dynamic Ron and causing drain current dispersion [12]. In HEMT operation, electron trapping occurs in several locations.

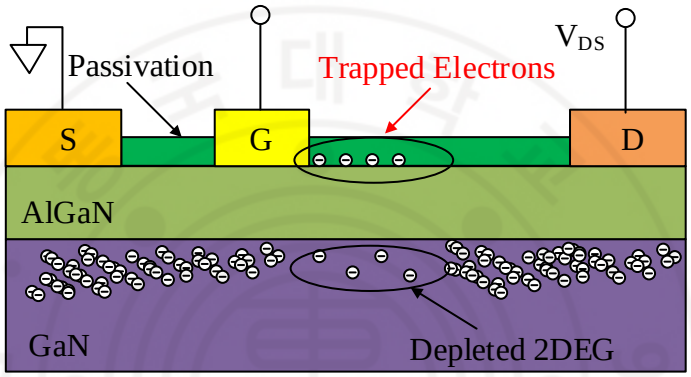

Figure 1. 3 . HEMT structure of an AlGaN/GaN device with trapped electrons i[12]

It has been determined that this effect is mostly caused by trapping at the surface, in the barrier layer AlGaN, at the two-dimensional electron gas (2DEG) interface, and in the buffer layer GaN. A large bias voltage applied between the source and drain accelerates electrons rapidly in a conducting channel, causing this effect. As the GaN buffer layer contains a concentration of traps, Trapped electrons can be injected into an adjacent region of the device structure.

All power semiconductor devices, on the other hand, are subject to thermal and self-heating effects. Electrons accelerate in random directions rather than following the drain to source channel due to self-heating of the device, especially when it works at high voltages and power levels. In Figure 1.2, electrons eject from the channel, causing a significant roll-off in the high-voltage and high-current regions.

Figure 1.4 shows a simplified diagram of a GaN/AlGaN HEMT.

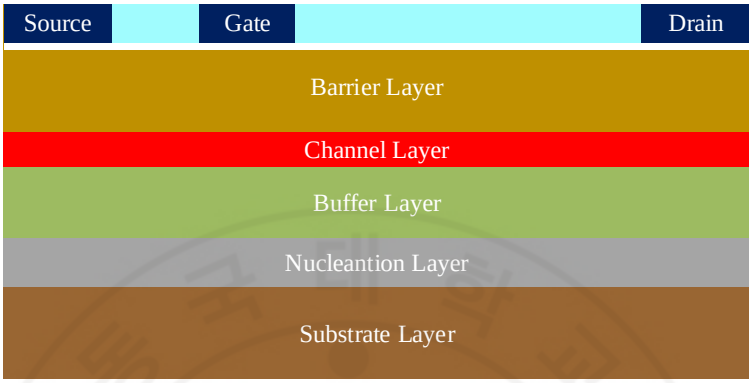

Figure 1. 4 Cross-Section of HEMTs (Not Drawn to Scale)

- Barrier: In this semiconductor layer, the gate is isolated from the channel, resulting in very little current flowing between them. GaN FETs typically use aluminum gallium nitride (AlGaN) as the barrier material.
- Channel: Electrons flow from the source to the drain through the channel, or 2-DEG. The channel is made from high-quality GaN.
- Buffer: Electrons are restricted from moving within the channel by the buffer. In this way, the buffer prevents electrons from wandering into the substrate. The buffer of a GaN FET is usually made of GaN doped with carbon (C) or iron (Fe).
- Nucleation: It is important that the GaN lattice is carefully matched to a foreign substrate during the formation of GaN structures on such substrates. Between the substrate and buffer layer, appropriate nucleation layers must be fabricated.

- Substrate: Substrates provide mechanical support, heat spread, and electromagnetic confinement. FETs based on GaN need a foreign substrate (such as Sapphire, SiC or Si). Due to the substrate not being GaN, the crystal lattice is different from that of the buffer. Therefore, dislocations occur in the material, which reduces the electrical isolation between the gate and the channel.

Despite remarkable advances in GaN growth and device fabrication, trapping effects remain a challenge and cannot be eliminated completely, which is still an active area of research in AlGaN/GaN HEMT applications. An accurate HEMT model that takes into account trapping effects is still required for developing AlGaN/GaN HEMT-based devices.

The second significant disadvantage of GaN HEMTs is their cost of fabrication. In order to commercialize power GaN HEMTs, reducing the production cost is crucial. Limited supply is a big barrier to commercialization. Today, it is possible to purchase GaN HEMTs from distributors due to the growing number of GaN device companies, but the variety is limited, and the price remains high compared to other technologies. Until interchangeable devices are available from multiple manufacturers, there is no high-volume use for GaN transistors among major manufacturers. In addition, due to the lack of bulk GaN source material, GaN had to be grown on substrates that were mismatched like Si, SiC and sapphire, which also results in poor quality epitaxial films with dislocation densities.

Second, GaN HEMTs are very expensive to fabricate. Reducing production costs is crucial for the commercialization of power GaN HEMTs. A major obstacle to commercialization is availability. Today, GaN HEMTs are available from a variety of distributors, but the selection is limited, and the prices remain high compared to other

technologies. GaN devices are being developed by an increasing number of companies around the world, so it is possible to obtain GaN HEMTs from distributors today. Furthermore, because the devices are not standardized between these distributors, no real second source of supply is available for them today. In high-volume applications, GaN transistors are unlikely to be used until interchangeable devices are available from multiple manufacturers. As a result of a lack of bulk GaN source material, GaN grew on substrates such as Si, SiC, and sapphire, resulting in poor quality epitaxial films with high dislocation densities.

1.3. Thesis organization

In this thesis, we investigate design techniques to attain high-performance and robust Rx path chips. Based on that, we demonstrate SPDT switch and LNA designs at X-band, with the oriented performance of high-power, high-efficiency, and area minimization.

Chapter 2 presents the theory of SPDT switch in TRx module, the outstanding characteristics of GaN which make GaN switch become one of the most favorite design in the market now. In this part, we present an X band SPDT switch using solely shunt transistors to switch and quarter-wavelength transmission lines in the signal paths improve isolation. Also, parallel inductors are utilized for matching purpose. The measurement setup and results will be shown to compare with simulation results, that verify the analysis in the design steps.

Chapter 3 introduces the design of proposed LNA. The LNA consists of 4 common source stages, the first stage is inductive source degeneration configuration for conjugate and noise matching purpose. RC-feedback is inserted in the final stage to improve stability and output matching. The Y-factor method, an accuracy method to measure NF also described detail in this chapter.

II. X-band 250nm GaN SPDT switch

2.1 Introduction

For the very high-power application, it is necessary to place a limiter ahead of the LNA to protect in GaAs front ends, which results in generating more noise for the system and complex the circuit as well (Fig. 3.1). A GaN monolithic microwave integrated circuit (MMIC) is feasible with high isolation, low insertion loss single-pole single-through switch that changes state between Rx and Tx. Using switches also significantly reduce the size of the module. GaN HEMT's high voltage operation and enhanced current density enable high power T/R switches to be designed for phased array applications. [13]- [15]

Despite of small size, simple structure of switch (when compared to LNA and PA), SPDT switch is placed right after antenna and connects both receive and transmit path. Thus, it demands a low insertion loss, while achieving high isolation. Exhibiting low insertion loss reduces signal degeneration on both paths, especially for the highly sensitive receive path, while high isolation minimizes signal leakage from Tx to Rx path in transmit mode. There are several approaches have been utilized in previous publications to increase the performance of SPDT switch. Power-handling ability can be greatly enhanced by using stacked-transistor [16]- [18].

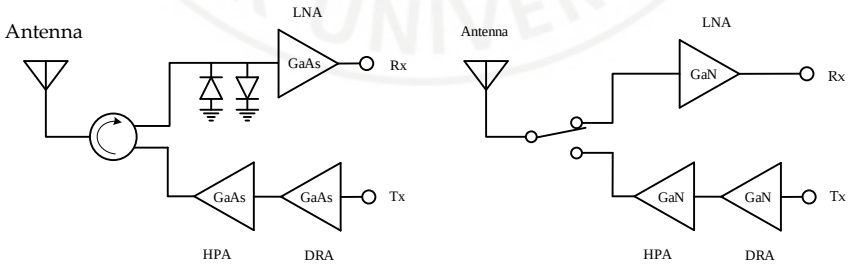

Figure 2.1 TRx system in GaAs and GaN technology

To learn more about the performance that GaN HEMT can provide, an SPDT switch is designed and fabricated. This switch is realized using lumped components and can cover X band. According to simulation results, the switch shows linear behavior approximately 40W RF incident wave. Moreover, this design's results are one of the best performances among the GaN switches available in literature based on insertion loss and isolation aspects.

2.2 GaN transistors as switches

RF switching can easily be accomplished with GaN transistors. Because they behave as voltage variable resistors, the drain-source resistance can be used for switch implementation. During a switch operation, zero volts DC are applied to the drain and source of the transistor. The RF Signals are routed from drain to source, with the gate serving as the control terminal.

In the region of V_{ds}=0V, the V_{ds}/I_{ds} characteristic approximates a resistance ($Ids \propto V_{ds}$). When Vgs=0V, the transistor is on with low drain-source resistance, and when Vgs is below pinchoff (typically around -3 to -5V for GaN processes), the transistor has high drain-source resistance. A simple approximate equivalent circuit is resulting from this, as shown below. A gate resistor (Rg) is used to provide isolation between the RF signal path and control port, a value of several kΩ is typically used. Parallel to the resistor, parasitic capacitance limits the isolation that the transistor can provide, and tolerating it is one of the fundamental challenges in the design.

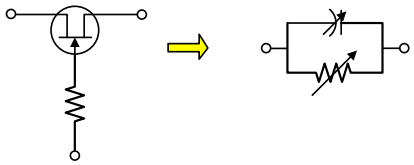

Figure 2. 2 Switch configuration

When used as a RF switch, GaN transistors are laid out differently than amplifying transistors. With GaN, switch transistors and amplifier transistors can be realized on the same die. The major difference between switch transistors and amplifying transistors is as follows:

- Through substrate vias, the amplifying transistors include integral grounded sources (connected to the back side of the die).
- In comparison with switch transistors, amplifier transistors have a larger gate finger pitch. As a result, the thermal performance (ability to dissipate heat) is improved, but the transistors take up more space on each die. It can tolerate a smaller gate pitch as a switch transistor normally dissipates less power than an amplifier transistor.
- In switch transistors, the gate is positioned between the source and drain. As a gate bias voltage, place it between the breakdown and pinch-off voltages for the process, this symmetric structure allows maximum RF power handling, with Vds=0V and in the off-state.
- Unlike field-coupled transistors, switch transistors do not have a source coupled field plate. RF performance is improved by reducing parasitic capacitances, but breakdown voltage is reduced. This may reduce the

breakdown voltage, but the control voltages are still impressively high, typically ranging from -25V to -40V.

RF GaN switches can be designed using a straightforward approach. SPDT switches typically use a single transistor in each arm, as shown below. V1 and V2 are complementary voltages (V1 is low when V2 is high, and vice versa). Despite its low loss, this topology offers limited isolation, which worsens with increasing frequency. The parasitic drain-source capacitance shown in the simplified equivalent circuit above results in a degradation in isolation. This SPDT's performance is greatly influenced by the transistor size (total gate width). It would be possible to reduce on case insertion loss by increasing the gate width of the transistor, but isolation would also be compromised. The switch is only suitable for use at low RF frequencies; more complex topologies are needed to extend the switch's performance up to microwave frequencies.

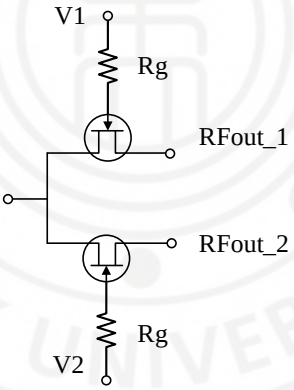

Figure 2.3 Simple series only SPDT

2.2 Design consideration

2.2.1 Design

Schematic of the SPDT switch is illustrated in Fig.2.4. It has symmetric structure; each arm consists of 4 parallel transistors which are connected by large transmission line. The on-state and off-state power handling capability of the SPDTs in a 50 Ω system can be predicted by using (2.1) and (2.2), [19].

$$P_{on} = I_{MAX}^2 . 25 \quad (2.1)$$

$$P_{off} = \frac{(V_{BD} - V_P)^2}{100} \quad (2.2)$$

From (2.1), the on-state power handling is limited by the maximum channel current (IMAX), the typical value for it at $V_{gs} = 0$ is about 1A/mm. Thus, the maximum available power can be through the series transistor is approximately 25W, which can be a threat for very high-power applications (usually 25W for recent designs). While, thanks to high band gap property of GaN, the break down voltage (VBD) has a very high value when compared to GaAs or CMOS. In specific, NP25-02 technology show the leakage current is lower than 0.1mA/mm under stress of V_{gd} is greater than 200V. Addition, with -2.6V pinch-off voltage (V_p), an off-mode HEMT can handle several hundred Watts.

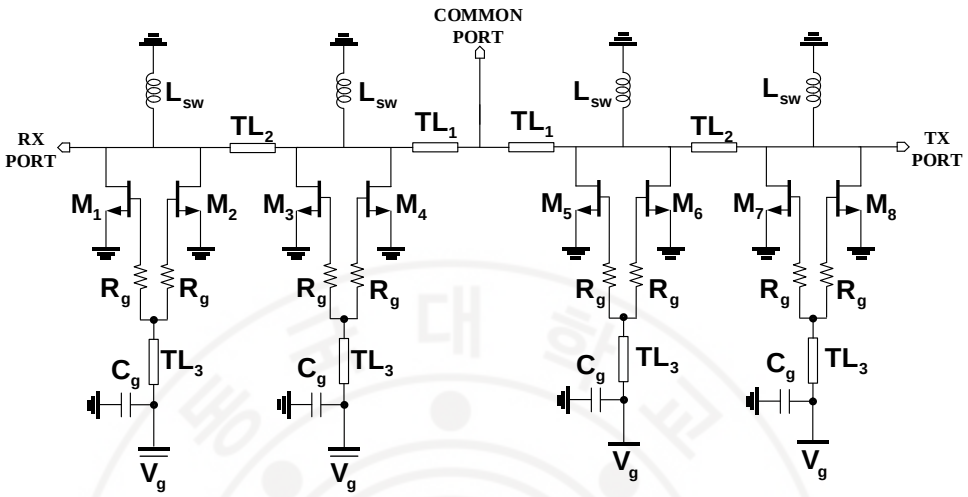

Figure 2. 4 Configuration of proposed SPDT Switch

With the demand of extremely high-power handling capability, signal paths are built on transmission line instead of series active devices. Be notice that these lines need to large enough to carry the level of input power as expected and considered the size issue. For the isolation, a quarter wavelength transmission line is used right at the antenna port. This line is calculated and tuned deliberately by using an electromagnetic simulator. The width and the length of TL1 are 100 μm and 3000 μm respectively in considering both insertion loss and the response at the band. While TL2 is tuned in considering size, isolation, and insertion as well.

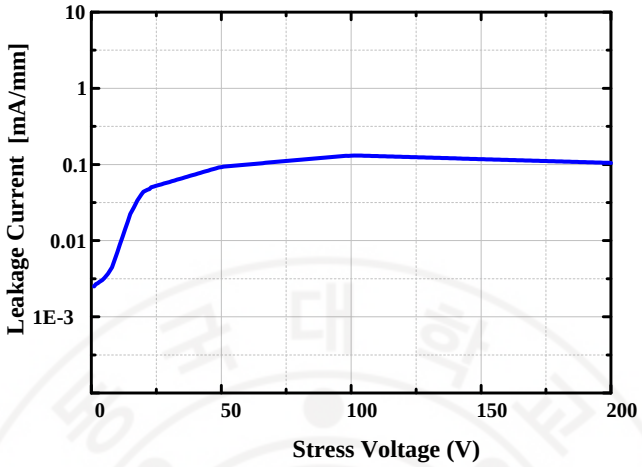

Figure 2. 5. Three terminal breakdown tests

As described in Fig.2.4, the switch is controlled by turning on/off transistors. Indeed, the signal from antenna and system is handled by transmission line entirely. As the design is symmetrical, the role of Tx and Rx are equal. The size of all shunt transistors is optimized to have the best insertion loss while provide good isolation and linearity. When Tx path is on, that means M1-M4 is turn on to translate leakage current from Tx to Rx to ground. Thus, they need to be large enough to dissipate wasted current, especially M3, M4. In consideration these aspects, the width of all transistors is 900 µm (9x100 µm). Shunt inductors are inserted to resonate with OFF-capacitance in the transistors off state, which can decrease the loading of the shunt transistor remarkable. In the ON state of shunt transistor, inductor is utilized as a matching component.

In this technology, the active devices are all depletion type, so by applying 0V control voltage would keep the transistor in the on-mode. While, in order to turn off transistor completely, a relative lower voltage than pinch-off voltage should be used. Moreover, thanks to low voltage control, the power handling capability will be improved significantly. Instead of using -40V as turn-off voltage control in most of publications, -

25V is chosen in this design, as it will be integrated with other blocks (e.g., LNA, PA,) to form transceiver system which use 25V for all blocks in this GaN technology

In most previous papers, a several k-Ohm resistors are used to decouple the circuit from the common gate ground [20]-[22]. From Fig 2.5, the leakage current can reach 0.1mA/mm, combining with a high value resistor generates a dozen voltage of shift in control voltage. This can make a huge variation in overall performance of switch, especially for transistors in on-mode as it can change state from on to off. Thus, in this paper, a narrow $\lambda/4$ transmission line is used at the gate line for isolating purpose. In addition, a 50-Ω resistor is inserted between the gate and line to enhance stability while not cause a large drop in voltage

The circuit and electromagnetic simulation are conducted in ADS software. In which, all transmission lines in the design are optimized based on 2.5D EM simulator. Fig 2.6 depicts the layout of the SPDT switch with the size of 3mm x 2.7mm

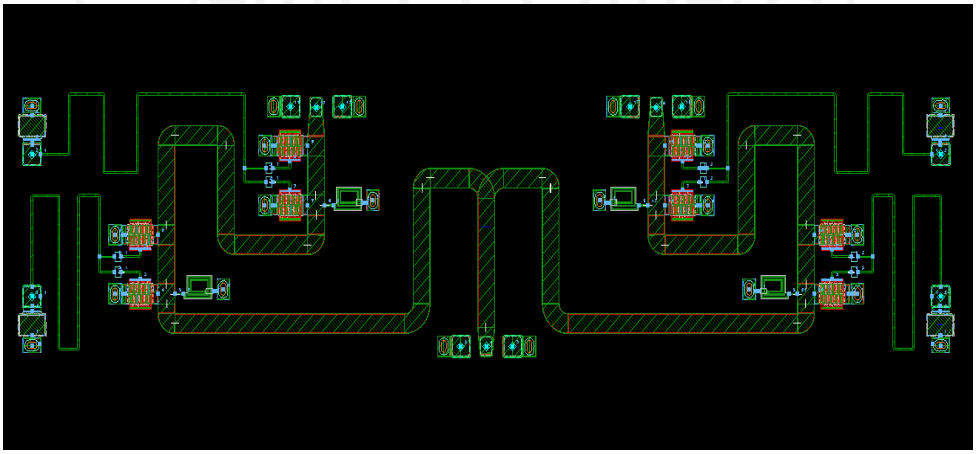

Figure 2.6. Layout of proposed SPDT Switch

2.2.1 Measurement

The chip is fabricated and measured within small signal measurement. For the large signal measurement, the IP1dB of the SPDT switch is 41dBm at 10GHz. Fig 2.7 shows the micrograph of the fabricated SPDT switch.

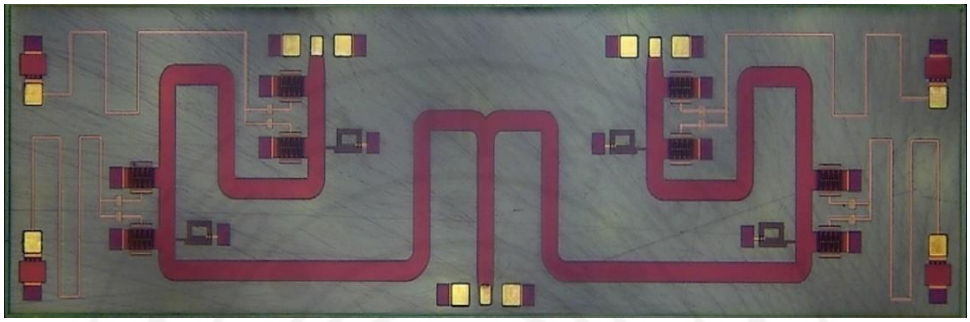

Figure 2.7 Photo of proposed SPDT Switch

With the balanced structure, Tx and Rx port are switchable in their role and results as well, so in this paper, the results are exactly same will not be shown.

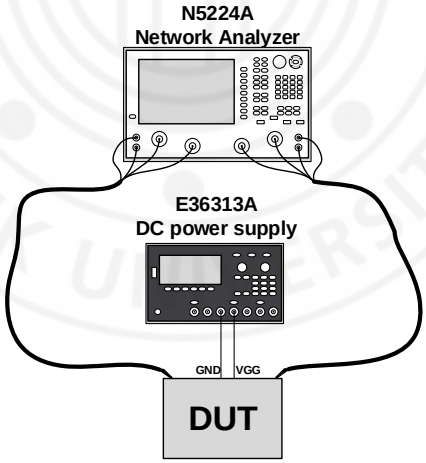

Figure 2.8. Setup for small signal measurement

Fig 2.8 illustrates how the SPDT switch is measured with small signal. The insertion loss results (simulation and measured) is shown in Fig 2.9. From that, the switch achieves 1.3dB insertion loss at X band and 1.2dB at 10 GHz.

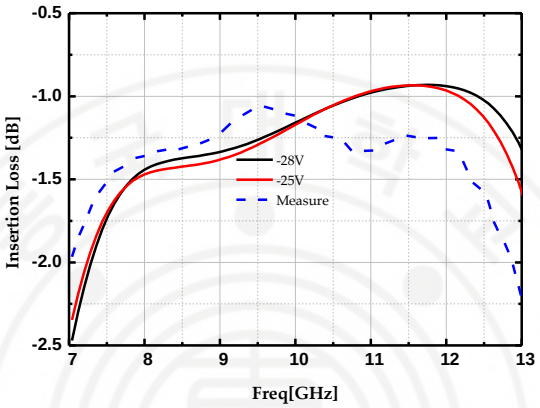

Figure 2.9. Insertion loss of proposed SPDT Switch

Fig 2.10 shows the measured return loss result of proposed switch, S_{11} is smaller than -10dB at X band. The trend of lines is same in simulation and measurement.

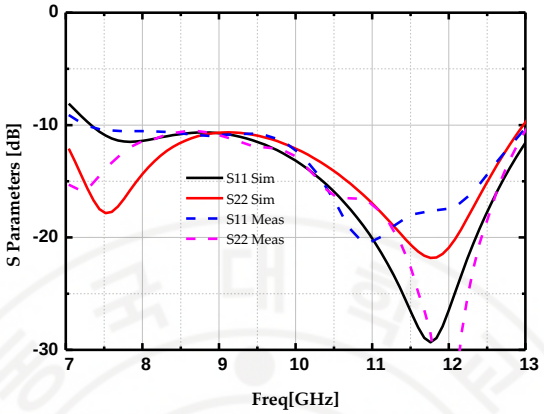

Figure 2. 10. Photo of proposed SPDT Switch

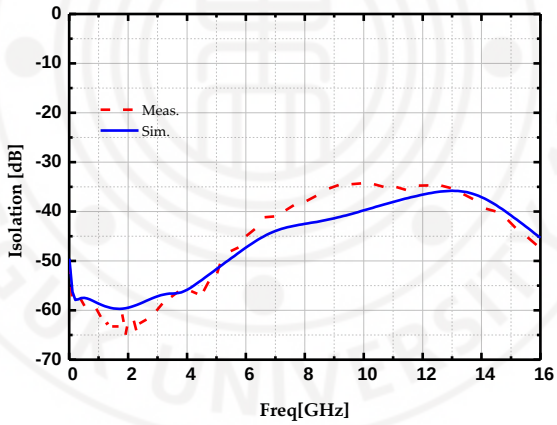

Figure 2.11. Isolation of proposed SPDT Switch

From Fig 2.11, isolation of the switch is better than 35dB at X band. Table 2.1 show the performance comparison of X band GaN SPDT switches measurement. It shows that the switch in this literature is one of the best performances among current designs.

Table 2. 1 PERFORMANCE COMPARISON OF X-BAND GAN SPDT SWITCHES

Ref.	[14]	[15]	[16]	[17]	TW
Process	GaN	GaN	GaN	GaN	GaN
Frequency (GHz)	0-12	2-18	8-12	3-13	8-12
Insertion Loss (dB)	< 1.0	2	1.4	1.7	1.3
Isolation (dB)	< 30	< 20	< 20	< 32	< 35
Power Handling (dBm)	42.5	35	38	39	41

III. X-band 250nm GaN Low Noise Amplifier

3.1 Introduction

GaN has developed quickly to become the newest star in the microwave-amplifier universe even though the market for high-gap materials has been dominated by GaAs for many years ago. Notably, with its low noise nature (thanks to high gm), GaAs seemly becomes an indispensable choice for low noise applications

Nonetheless, it is necessary to place a limiter ahead of the LNA to protect in GaAs front ends, which results in generating more noise for the system and complex the circuit as well (Fig 2.1). GaN-based HEMTs with very high-power density, high breakdown voltage has the ability to provide a complete transmit-receive solution. An MMIC is feasible with high isolation, low insertion loss single-pole single-through switch that changes state between Rx and Tx. Using switches also significantly reduce the size of the module.

For low noise, wideband applications, some structures have been introduced distributed with non-resistive termination [23], RC-feedback, inductance degeneration [24]. However, RC-feedback will generate high NF (normally above 3dB), inductance degeneration depresses the total gain.

3.2 The design of LNA

For the high-power application, even though with inherent robustness of the fabricated process, GaN LNA also witness a degradation when the voltage swing at the gate is high enough that make it becomes forward biased for a while. To overcome this phenomenon, a big resistor is attached at the gate biased [25]. This also aids in keeping the gate current under control

Choosing active devices becomes the first-tough work for any RF circuits. In this design, the HEMTs for the first stage must be chosen deliberately as it manages the input matching and almost noise figure of the total LNA. As can be seen from (3.1), the total noise factor is mainly from the first stage amplifier and somewhat from the gain booster. Fig 3.1 depicts LNA blocks with 4 stages.

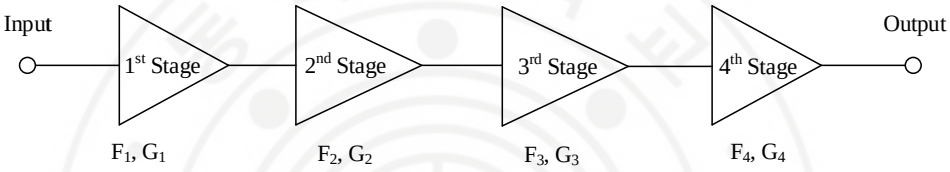

Figure 3. 1 Block diagram of the proposed LNA

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} \tag{3.1}$$

The schematic of the design is depicted in Fig 3.2. It comprises 4 common source stages. The first stage uses inductor in the source to configure degeneration structure that can match noise and conjugate matching simultaneously. At the 2 final stages, an RC feedback is used for stability purpose.

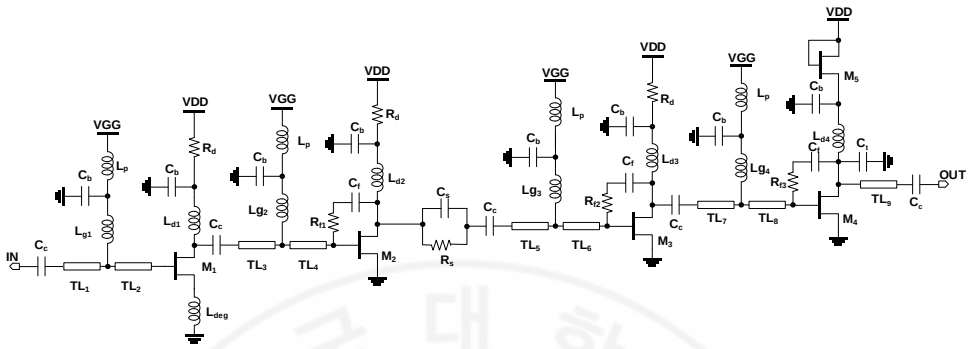

Figure 3.2. Schematic of proposed LNA

Fig 3.3 shows the NF_{min} dependent on the bias condition of the 200μm unit cell transistor for a 10V drain voltage. These results are measured and provided through noise models. In concern to power consumption and noise performance, and also linearity, a bias current density of ~ 100mA is used in this design. It should be emphasized that NF_{min} is more appropriate for narrow-band LNA designs, where NF min can be obtained by providing the device with the best source impedance. Nonetheless, the basis bias dependence and device size with respect to Γ_{opt} can provide significant insight for improving the LNA design over a wide frequency range.

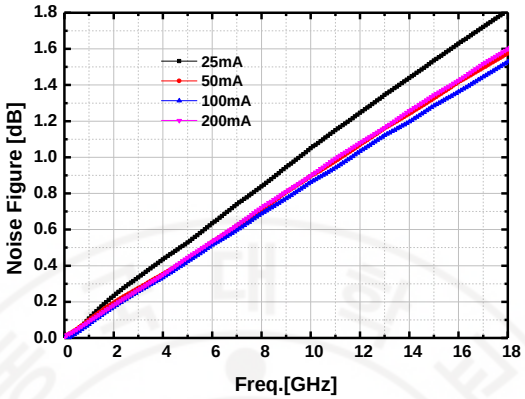

Figure 3.3. NF of 4x50μm HEMT with different bias conditions

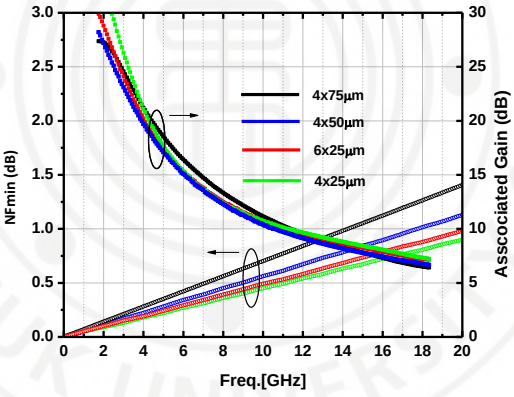

Figure 3. 4. NF and associated gain of 4 different devices

All the transistors in this circuit are biased with $VDD = 10V$, $Idss = 100mA/1mm^2$ which ensures $I_d = 100mA/mm$ follow the measured noise value provided by the vendor. It also brings a good trade-off between small-signal gain and usage of energy.

Low drain voltage results in the gain would be too small. A small resistor R_d has been used at the drain to stabilize the circuit

Instead of using inductors for the signal path, transmission lines with a width of 50μm are realized for transmitting signal and matching purposes as well. The maximum current is 307 mA. This not only reduces the loss of wires also makes the circuit more reliable in very high-power applications. On the other hand, these lines have high cut-off frequency results in it easy to achieve a wide band. In previous GaN works, stabilization has been made by using RC feedback, source degeneration, or cascade configuration. Although these techniques are beneficial for bandwidth, noise figure, likewise they degrade gain performance significantly. By using transmission lines ingeniously, the structure in this work maximizes available gain, while still having a good noise and bandwidth.

3.3 Measurement

3.3.1 Noise Figure Measurement

This application note describes how to measure noise figure using a spectrum analyzer using the Y factor technique. A broadband noise source characterized by two temperature states is used in this technique: In a high-temperature state, T_{source}^{ON} with a greater output of noise power, and in a low-temperature state, T_{source}^{OFF} with a reduced output of noise power. The DUT input is applied with the noise source, and the output noise power is measured for each of the two input noise states. These measurements are used to calculate the noise figure and gain of the DUT.

Figure 3.5 shows a typical setup for measuring noise figures. A spectrum analyzer and a noise source are needed. Spectrum analyzers often come with a built-in preamplifier. Integrating a 28V DC port is a convenient addition to the spectrum analyzer

and facilitates measurement automation. The DC power supply is used to switch the noise source between its hot and cold states.

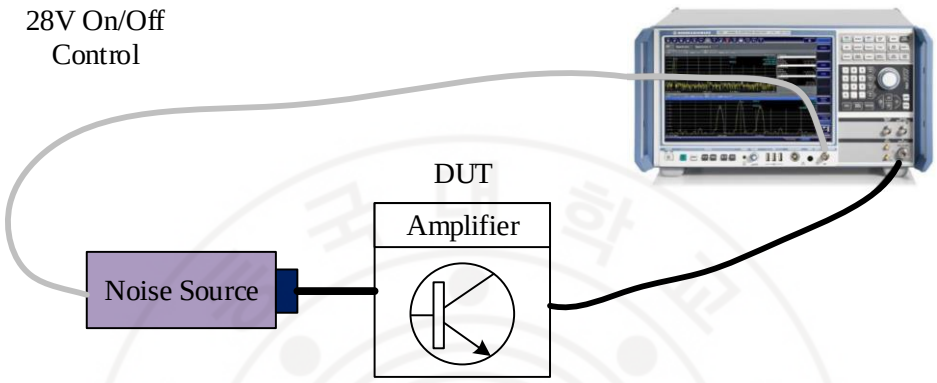

Figure 3.5. Common setup to Measure Noise Figure

The DUT gain, G_{DUT}, can be calculated using two measurements. The Y-intercept represents the noise added by the DUT, N_{DUT}. In Figure 3.6, B, the bandwidth (in Hz) of the noise measurement, and k (1.38 x 10-23 Joules/˚K), are also shown.

Manual noise figure measurements with spectrum analyzers require conversions between noise figures, noise factors, noise temperatures, linear gain, log gain, linear power, and log power. Here are the equations needed for these conversions

Assuming a linear power, P, in units of watts, the first conversion requires the linear power to be expressed as a log power. All log powers will be in units of dBm, which is a ratio of the linear power to 1 mW

$$P_{dBm} = 10\log\left(\frac{P}{0.001}\right) \tag{3.2}$$

The inverse relationship converts a log power "P_{dBm}" to a linear power with units of watts

$$P = (0.001) \cdot 10(^{P_{dBm}}/_{10}) \tag{3.3}$$

In a similar way, linear noise factors "F" is converted to log noise figures:

$$F_{dB} = 10(^{F_{dB}}/_{10}) \tag{3.4}$$

Noise Figure (log) is related to Noise Temperature by equation (3.5)

$$T_{DUT} = T_0(10(^{F_{dB}}/_{10}) - 1) \tag{3.5}$$

Where T_0 is the ambient temperature of the DUT. Noise Temperatures use the Kelvin scale. The inverse equation follows as:

$$F_{dB} = 10\log(\frac{T_{DUT}}{T_0} + 1) \tag{3.6}$$

Decibels (dB) are commonly used to describe the excess noise ratio of noise sources. This relationship is shown by equation (3.7). Typically, noise source manufacturers provide calibrated ENR values based on T_0 = 290K

$$ENR_{dB} = 10\log(\frac{T_{source}^{ON} - T_{source}^{OFF}}{T_0}) \tag{3.7}$$

ENR is then converted into an "on" temperature by:

$$T_{source}^{ON} = T_0(10^{\left\lfloor \frac{ENR}{10} \right\rfloor}) + T_{source}^{OFF} \tag{3.8}$$

Here are the remaining equations related to the Y factor method. When using the Y factor method, a measurement of the noise power at the DUT output is made with a room temperature noise source at the input (noise source off), and a measurement of the noise power at the input with a high temperature noise source (noise source biased at 28V).

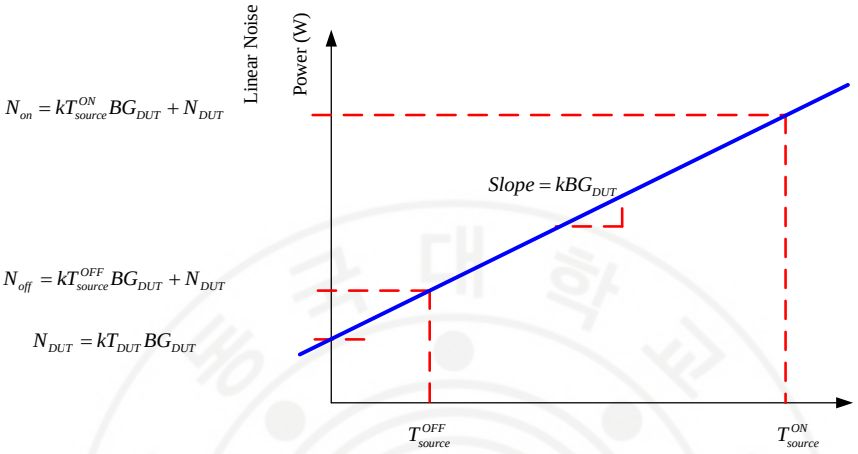

Figure 3.6. Diagram showing the Y factor variables

When the noise source is turned on, measure the (linear) noise power at the DUT output compared to when it is off and then calculate the Y factor term.

$$Y = \frac{N_{on}}{N_{off}} \tag{3.8}$$

The noise temperature of the DUT can be calculated using the Y factor with the following equation:

$$T = \frac{T_{source}^{ON} - Y \cdot T_{source}^{OFF}}{Y - 1} \tag{3.9}$$

Spectrum analyzer noise figures (or linear noise factors) can be characterized and deducted from the overall measurement using the cascaded noise factor equation in many cases. Calibration or second stage correction is often referred to as this. The error in the second stage is negligible when a low noise figure spectrum analyzer is used with a high

gain and high noise figure DUT. Most of the time, however, a second stage correction is recommended. Cascaded noise figures are expressed linearly by equation (3.10).

$$F_{DUT\&SA} = F_{DUT} + \frac{F_{SA} - 1}{G_{DUT}} \tag{3.10}$$

Noise figures for the spectrum analyzer and the cascade are both measurable. The gain of the DUT can be represented with the following linear equation:

$$G_{DUT} = \frac{N_{on}^{DUT\&SA} - N_{off}^{DUT\&SA}}{N_{on}^{SA} - N_{off}^{SA}} \tag{3.11}$$

To figure out the noise temperature of the DUT, we use equation (3.12) based on the gain of the DUT and the noise temperature of the second stage (the spectrum analyzer).

$$T_{DUT} = T_{DUT\&SA} - \frac{T_{SA}}{G_{DUT}} \tag{3.12}$$

Combining equations (3.6), (3.7), and (3.9) yields equation (3.13), which is a simplified version of the noise figure equation.

$$F_{dB} = ENR_{dB} - 10\log(Y - 1) \tag{3.13}$$

Where Y is the measured Y factor as a linear ratio

3.3.2 Measurement Results

Fig 3.7 shows the comparison between simulation and measured results in S-parameters of the proposed LNA. The 3dB-bandwith is from 8-11GHz with the peak gain is 29.5dB at 9.5GHz. The input and output return loss are also better than 10dB at such frequency span. The trend of lines is pretty same with 0.5GHz shift frequency.

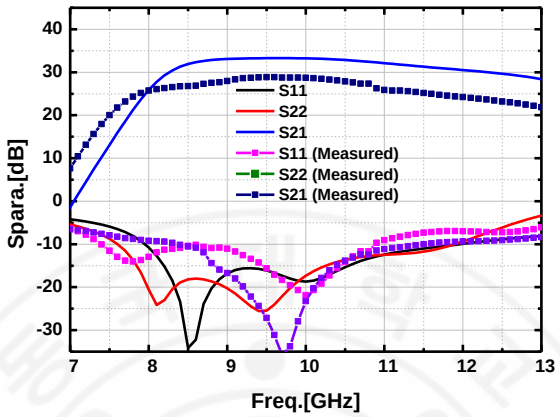

Figure 3.7. Measured and simulation S-parameters results of LNA

The large signal measurement also is conducted to check the output power of this LNA. From the initial spec, the proposed LNA should not provide output power exceed 25dBm to protect the behind circuit. This can be made by using diode-connected at the drain line of the final stage, it operates like a limiter. It can be seen from Fig 3.8, it shows the output power of the switch at 10GHz, the saturated output power is 20.5dBm and the IP1dB is -14dBm.

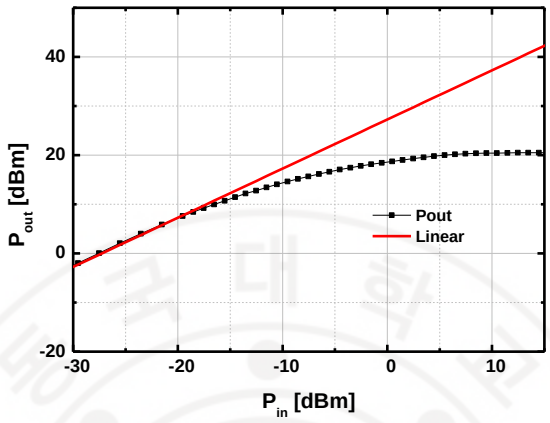

Figure 3.8. Measured output power at 10GHz

The NF results are shown in Fig 3.9 with comparison between simulation and measured results. The measured NF is higher than simulation one a bit with NF at 10GHz is 2.1dB, and the average NF at X band is 2.5dB. The results is measured follows the setup in Fig 3.10 and Y-method factor that described in section 3.3.1.

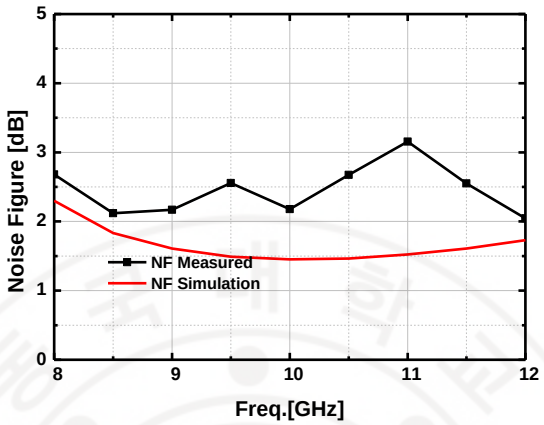

Figure 3.9. Measured NF of proposed LNA

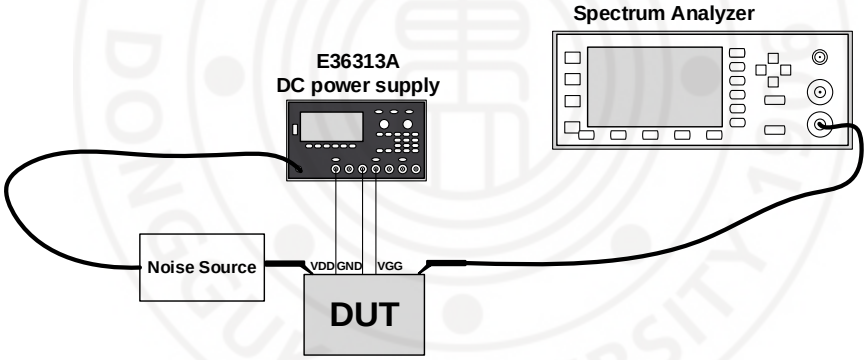

Figure 3.10. Setup for NF measurement

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