Dissertation for the Degree of Master of Engineering

An X-Band Bi-Directional Transmit/Receive Module for a Phased Array System in 65-nm CMOS

Advisor: Professor Jung-Dong Park

Van-Viet Nguyen

Department of Electrical and Electronic Engineering

Graduate School

Dongguk University

2019

Dissertation for the Degree of Master of Engineering

An X-Band Bi-Directional Transmit/Receive Module for a Phased Array System in 65-nm CMOS

by

Van-Viet Nguyen

Advisor: Professor Jung-Dong Park

Date of submission : 2018/12

Date of approval : 2018/12

Approved by:

Chairman : Professor Hyun-Chang Park (Sign)

Committee member : Professor Jin-Woo Jung (Sign)

Committee member : Professor Jung-Dong Park (Sign)

Department of Electrical and Electronics Engineering

Graduate School

Dongguk University

2019

ACKNOWLEDGEMENTS

First and foremost, I would like to express my sincerest gratitude and thank my advisor Prof. Jung – Dong Park for the continuous support during my Master study and research at his lab, for his patience, motivation, enthusiasm, and immense knowledge. His guidance helped me both in doing research, writing paper, and thesis as well as my life in Korea.

I also especially thank my senior Hyohyun Nam for his major help and significant contribution in my research. I would like to thank my lab mates Van-Son, Chen, Young Joe, and Jeong Moon for the time we were working together and all the fun we have had in the last two years. I feel a sincere gratitude to all my Vietnamese friends in Korea, we were sharing a lot of wonderful moments over two years.

Last but not least, I would like to thank my family: my parents, my sisters for their constant encouragement throughout two interesting and challenging years. I must express my very profound gratitude to my girlfriend for her sacrifice, unconditional support and love, and recovering me whenever I think of giving up. This accomplishment would not have been possible without them. Thank you.

Van – Viet Nguyen

Seoul, Korea, November 15, 2018

ABSTRACT

This thesis mainly presents an X-band bi-directional transmit/receive (T/R) module for a phased array antenna system in 65nm CMOS. The chipset is comprised of a 6-bit digital phase shifter, a 6-bit digital attenuator, and bi-directional gain amplifiers (BDGAs). The phase shifter has the coverage of $360°$ with the minimum phase shift of $5.625°$ while the attenuator can vary from 0 to 31.5 dB with the step of 0.5 dB. The circuit achieves the reference-state gain of 3.7 dB and the return loss of better than 11 dB at 8-12 GHz. The T/R module in all phase shift states has RMS phase errors of less than 4° and RMS amplitude errors of less than 0.93 dB from 9-11 GHz. In all attenuation states, its RMS amplitude and phase errors were less than 0.5 dB and 8° from 9-11 GHz. The output P1dB of the design is about 5.13 dBm at 10 GHz. The chip occupies an area of $3.74 \times 1.35\, mm^2$ and consumes the DC power of 170 mW mainly in BDGAs.

ABBREVIATIONS

BDGA	Bi-directional gain amplifier
DPDT	Double pole double throw
SPDT	Single pole single throw
NF	Noise figure
RMS	Root mean square
IL	Insertion loss
T/R	Transmit/receive
AESA	Active electronically scanned array
PDK	Process Design Kit
P1dB	Power 1-dB Compression Point.
TRM	Transmit/Receive Module

Table of Contents

LIST OF FIGURES

LIST OF TABLES

Chapter 1 INTRODUCTION

1.1 Introduction about phased array system

A phased array is also known as an electronically scanned array; a computer-controlled array of antennas [1]. It has an ability to form a radio-wave beam which can be electronically steered to different directions in space without mechanically moving the antennas. Due to the capability to electronically control and rapidly scan the radio-wave beam, phased array systems have been widely employed in defense and commercial applications [2]. Basically, phased array systems were first invented to serve in military radar systems, taking advantage of its electronical beam control and rapid beam scanning to quickly detect aircraft and missiles across the sky [3]. These phased array radar systems have now dominated the market of military equipment and phased arrays are spreading to civilian applications.

The origin of phased array technology is marked since the directive wireless communication invented by Nobel laureate Karl Ferdinand Braun [4]. Although transmission of radio waves in one direction had been explored and developed, there was still an issue that is, in fact, the radio signal received did not come from a certain direction, but its direction changes. Emerging as a practical solution to the above issue, the phased array antenna system which has a capability to steer the radio-wave beam to point in different directions has been established and improved.

Regarding the applicable areas of phased arrays, this technique has been originally deployed in military radar systems for many decades. Phased array radars provide a capability to use a single radar system for detection and tracking on land and air (detecting aircraft and missiles) and missile uplink capabilities [5]. Another potential application which can greatly benefit from phased array systems is collision avoidance radar for automobile or adaptive cruise control technology [6]. Phase array can also play a crucial part in the success of many commercial applications such as

gigabit wireless communication systems at 60 GHz, recent satellite TV systems and biomedical applications such as RF imaging for breast cancer detection [7].

1.2 Basic theory about the phased array system

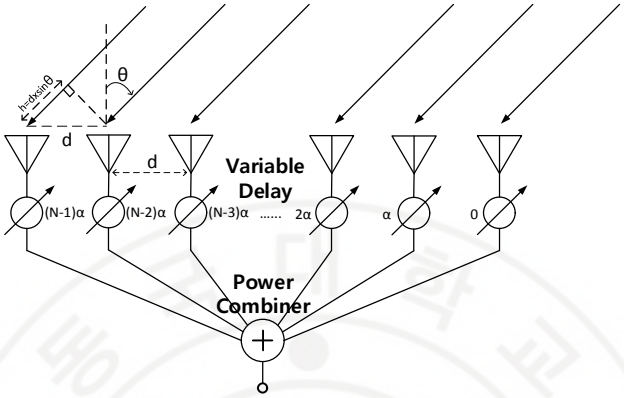


Figure 1.2-1 Simple diagram of an N-element phased array system.

Figure 1.2-1 illustrates the simple diagram of an N-element phased array system in which "N" identical unit antennas are located equally in space with a distance "d" between two adjacent elements. The case mentioned here is for receiver part while similar concepts can be applied for the transmitter as well. Variable time delays are integrated into each signal path of the phased arrays to separately control the phase of the signals. The signals received at each antenna element after passing through variable time delay blocks are summed up at power combiner block. It is assumed that the plane-wave beam of incidence arrives at the antenna arrays at an angle of θ to the normal direction. Due to the different position in space, the phase delay between two adjacent antennas to receive the signal is expressed in below equation:

$$\Delta\tau = \frac{2\pi d sin(\theta)}{\lambda} \qquad (1.1\text{-}1)$$

Where λ is the wavelength of the signal. Thus, if the plane-wave beam is assumed to be a sinusoid with ω and A as frequency and amplitude respectively, each antenna element will receive the signal in the form expressed as Equation (1.1-2).

$$X_i = Ae^{-jn\Delta\tau} \tag{1.1-2}$$

As mentioned above, the plane-wave beam of incidence arriving at the phased arrays suffers a linear phase delay throughout the array of antennas. Hence, to synchronize the signals before passing power combiner block, the variable delay circuits should also be configured linearly but in reverse trend. Subsequently, the form of the signal at the output of variable phase delay blocks can be shown in Equation (1.1-3).

$$X_i' = Ae^{-jn\Delta\tau}e^{+jn\alpha} \tag{1.1-3}$$

Here, α is known as the phase shift step between two adjacent variable phase delay elements. The array factor which is defined as the summation of all the signals normalized to the amplitude of the incident signal can be written as Equation (1.1-4):

$$F = \sum_{n=0}^{N-1} e^{-jn(\Delta\tau-\alpha)} \tag{1.1-4}$$

It can be easily observed that the maximum of the array factor happens when the phase delay blocks integrated into each path provide exactly the same amount of leading phase to compensate the delay of received signals. The incident angle in this case called scan angle can be determined by Equation (1.1-5) as below.

$$\frac{2\pi d}{\lambda}\sin(\theta^*) = \alpha \tag{1.1-5}$$

Resulting in

$$\theta^* = \sin^{-1}\left(\frac{\lambda\alpha}{2\pi d}\right) \tag{1.1-6}$$

Substituting expression of time delay $\Delta\tau$ into array factor equation, it becomes:

$$F = \frac{\sin^2\left[\frac{N}{2}\left(\frac{2\pi d sin(\theta)}{\lambda} - \alpha\right)\right]}{\sin^2\left[\frac{1}{2}\left(\frac{2\pi d sin(\theta)}{\lambda} - \alpha\right)\right]} \tag{1.1-7}$$

When the incident angle approaches the scan angle "θ^*", the array factor reaches a maximum value of N^2. According to the above equations, there are three important observations. First, moving far away from the scan angle θ^*, the array factor becomes smaller than the peak value demonstrating the spatial selectivity of the phased arrays. Second, the expression of the scan angle in Equation 6 reveals that it is possible to electronically tune the variable time delay elements to satisfy the condition for maximizing the array factor, without any mechanical interact to the phased arrays. Third, basing on the fact that the array factor approaches the maximum value of N^2, then the performance of the phased array system can be greatly improved by increasing the number of elements.

1.3 The proposed T/R module for active phased array systems

In recent years, Active Electronically Scanned Arrays (AESAs) with rapid development has gradually replaced the mechanically scanned tube in today's and future radar systems [8]. Transmit/receive modules (TRMs) play the most important roles in active phase array antennas employed in many radar and electronic warfare applications [9,10]. Currently, GaAs pHEMT (pseudomorphic High Electron Mobility Transistor) devices are used in most commercialized TRMs[11,12]. Moreover, TR modules have also been reported in the SiGe BiCMOS process [13-17]. Though high RF performances can be achieved, relatively high power consumption and production cost make them less attractive. The fact is that an AESA system requires thousands of TRMs, thus, to significantly lower the cost of an array system aiming to low-cost commercial applications, the production cost of a single TRM has to reduce accordingly. Recently, the advanced innovations in silicon technology enable to implement T/R modules on a standard CMOS process, which will bring the benefits of lower fabricating cost and higher integration [18,19]. Typically, the agile control of phase and amplitude are the key features of CMOS T/R modules to accurately steer the antenna beam [20,21]. Therefore, three main

components in a TRM are phase shifter, attenuator, and bi-directional gain amplifier (BDGA). The BDGA is needed to compensate the losses caused by CMOS switches integrated in passive control blocks [22,23]. Implementing TRMs in standard CMOS technology brings many advantages and is still a challenging task, especially in solving the problem of MOS device switch losses. More effort has been put into improving the performance of MOS switches via maximizing or minimizing the substrate resistance [24-26] and via using the body-floating technique [27,28]. The proposed TRM employs double-well body-floating technique in single-pole-double-throw (SPDT), and double-pole-double-throw (DPDT) switches used in phase shifter and attenuator to reduce losses and enhance power handling capability [29,30]. The proposed TRM has been realized in 65 nm CMOS process with 1.2 V of supply. Chapter 2 presents a general view of functional blocks in a TRM. The detailed design procedure with corresponding simulation results of the X-band CMOS TRM is described in Chapter 3. The experimental setup and measurement results of the implemented TRM (called Design 1) are also presented in this chapter. Chapter 4 introduces Design 2 of the TRM with the new structure of BDGA where gain boosting stage and asymmetric cell topology are applied to enhance gain and output power of the entire system. The simulated result comparison of Design 1 and Design 2 are fully provided.

Chapter 2 DESIGN CONSIDERATION OF FUNCTIONAL BLOCKS

2.1 The 6-bits Phase Shifter

2.1.1 General perspectives of the phase shifter

The phase shifter is the key element employed in phased array systems. Its phase shift capability needs to be adequate to steer the radio – wave beam and achieve good spatial selectivity. There are some constraints for designing a phase shifter such as 360° coverage, small insertion loss, sufficient bandwidth, power handling and linearity, low power consumption and small size. The present of inductors is indispensable to a phase shifter design making it the more area consuming block in the whole chip. The control mechanism is also an important aspect need to be considered, and simplicity is preferred. In addition, the variation of amplitude depends on different phase setting is one of the performance indicators, which should be the smaller, the better. Finding out the appropriate tradeoffs for a specific application is a challenging task for designers in phase shifter designs. As many other functional circuits, either active or passive potential solutions have been found including phase shifter with varactor-tuned transmission lines, reflective type phase shifter, a phase shifter with vector modulators, and digitally bit-controlling phase shifter.

2.1.1.1 Phase shifter with varactor-tuned transmission lines

As demonstrated early in [31], by adjusting transmission line, phase controllability can be achieved. The idea behind the method described in this subsection is that we can replace transmission lines with equivalent lumped elements which occupy less chip area but still gives phase control capability. High pass/low pass filter networks either in T or Pi configuration are usually utilized in this type of phase shifters. Widely used than others, Pi-type low pass filter network which needs

least inductors gives the benefit of small chip area. Figure 2.1-1 shows the simplified circuit structure of varactor-tuned transmission line (TL) phase shifter.

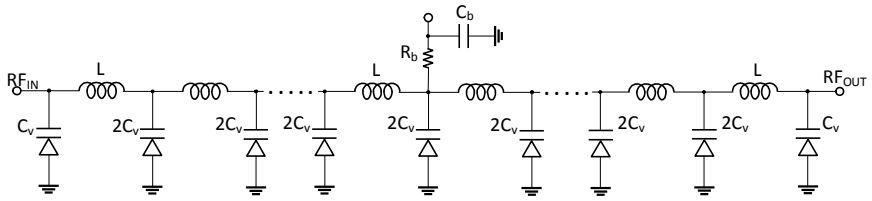


Figure 2.1-1 Simplified structure of varactor-tuned TL phase shifter.

2.1.1.2 Reflective type phase shifter

Reflective line phase shifter [32] is made up of a branch-line coupler ($3dB$ 90° hybrid coupler) terminated by a pair of reflective loads with identical impedances Z_r as illustrated in Figure 2.1-2. The demanding characteristic of the branch-line coupler is that its two coupled arms must be shared an identical power split (3dB split) and the phase difference between them must be 90°. With these characteristics, the incoming signal gets divided equally into two halves which then reflect off a pair of symmetrical loads and finally merge together in phase at the output port of the phase shifter if the reflection coefficient at loads are identically kept (easily to see that each half of the input signal goes through equal paths). Noted that if the reflective loads are assumed to be purely reactive, there is no power loss on them and total signal power is delivered to the output port. The noteworthy feature of this structure is the preservation of impedance matching at input and output ports despite the coupler terminated by the reactive load that is to say the coupler acts as an impedance isolator.

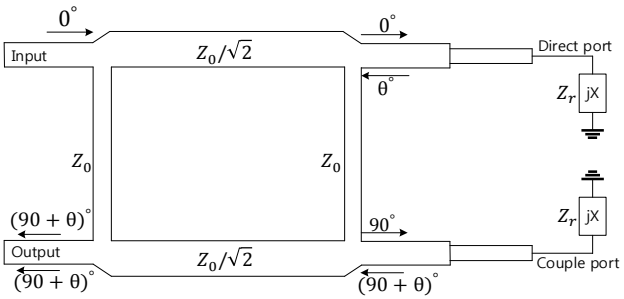


Figure 2.1-2 The simplified structure of a reflective type phase shifter.

2.1.1.3 Vector modulators

A vector modulator can also be utilized to perform phase shifting function, with an additional advantage of amplitude control [33]. The incoming signal is split into two parts which are then passed through separated variable gain amplifiers or attenuators. After being amplitude-weighted, a phase offset is created between these two signals in many ways such as a 90° hybrid. Finally, the two signals are re-combined by a combiner at the output port as can be seen in Figure 2.1-3 .

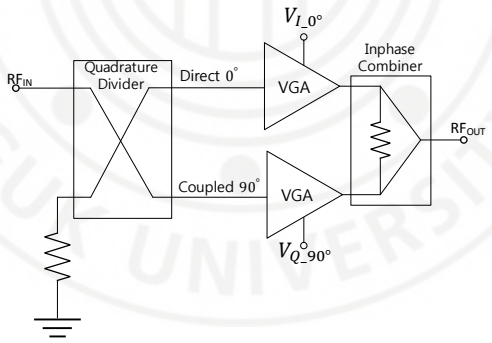


Figure 2.1-3 The simplified structure of a 90° vector modulator.

A vector diagram as shown in Figure 2.1-4 can be used to illustrate the generation of expected phase. For instance, if the peak amplitude is set for the 0° path and lowest one for 90° path, the phase of the output signal is 0°. Contrastingly, the output phase of 90° can be obtained by the opposite setting. Especially, when both paths carry identical amplitude signals, the phase of 45° is generated at the output. Similarly, for

the case of employing a 90° hybrid, every phase within the interval between 0° and 90° can be reached by setting an appropriate amplitude for each signal paths. It is noticeable that to obtain constant amplitude at the output, proper amplitude setting for each branch is required. For example, if both branches of the coupler are fed with maximum amplitudes to form a 45° phase shift, the result signal's amplitude would be higher than in cases of 0° and 90° by a factor of $\sqrt{2}$, which is not acceptable. However, if the adjustment range for the amplitudes is within 1 in 0° and 90° cases, and within $1/\sqrt{2}$ in 45° case, achieving constant amplitude of output signal becomes possible.

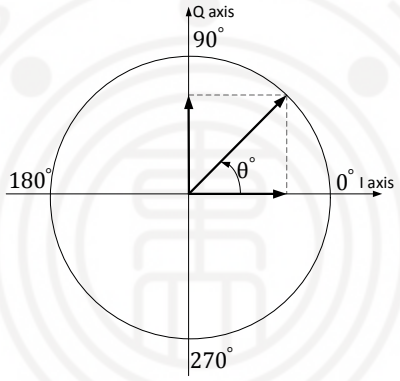


Figure 2.1-4 A typical vector diagram.

To provide the phase coverage of 360°, there are several solutions to choose the number of divided paths and accordingly, the phase offset between two paths. For instance, it requires 4 paths with 90° phase offset each or 3 paths with 120° phase offset each. Wide phase control ranges need a large phase offset while increasing phase offset results in decrease output amplitude, especially towards 180°. To make a compromise between phase shift range and level of output amplitude, a system with a phase offset of 120° can be chosen. It needs just three splitting paths and control voltages, enabling to reduce circuit size and complexity.

2.1.1.4 Digitally bit-controlled phase shifter

All the above-mentioned types of phase shifter are categorized as analog phase shifters, which show the significant advantage of high phase states density. It is due to the fact that with analog voltage control mechanism, every phase shift value can be reached, assuming that the resolution of the ADC is sufficiently high. In addition, the drawbacks of this approach are a high requirement of power consumption and the demand for control purposed ADCs which will increase the cost of the system significantly. As being applied in some functional circuits (such as attenuators) the topology in which the phase shifter circuit consists of several unit elements, each element provides a certain amount of phase shift. The role of costly ADCs in the above circuits is replaced by "digitally" bit-controlled mechanism which requires just digital high or low voltage levels. By setting the control bits, the signal can be arranged to pass through specific phase shift elements to achieve the desired phase shift at the output. There are several ways to implement phase shift units including delay lines or high pass /low pass filter networks with lumped elements.

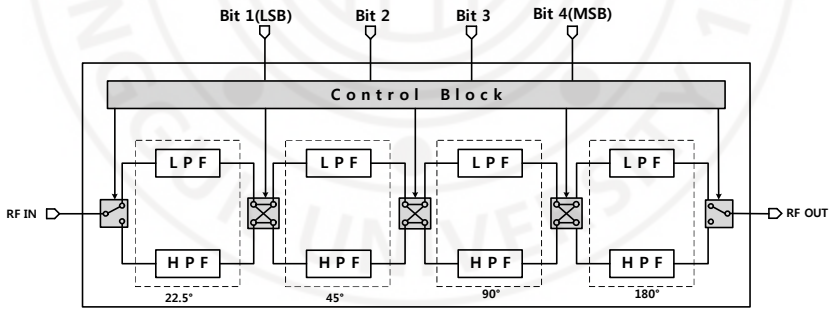


Figure 2.1-5 The block diagram of the digital phase shifter with 4 bits resolution.

Figure 2.1-5 sketches the block diagram of a 4 bits phase shifter. It has the coverage range of 360° and the minimum step phase shift determined by least significant bit which is 22.5° in this case. It is easy to observe that a design with high phase resolution also comes with high overall insertion loss and large circuit area.

2.1.2 The design choice for the phase shifter

Phase Shifter is the key element of phased array antenna system. Its phase shifting capability need to be adequate to steer array pointing beam. There are four types of a phase shifter including switched line, reflection, loaded line and high-pass/low-pass phase shifter. In recent year, high-pass/low-pass (HP/LP) network phase shifter has become popular because of its advantage in power, digitally control capability and broadband operation. The basic concept of HP/LP phase shifter is that a high-pass filter made up of series capacitors and shunt inductors provide phase advance while a low-pass filter constructed by series inductors and shunt capacitors produces phase delay. By applying a switching mechanism between low-pass and high-pass sections, the circuit can function as phase shifter with wideband performance.

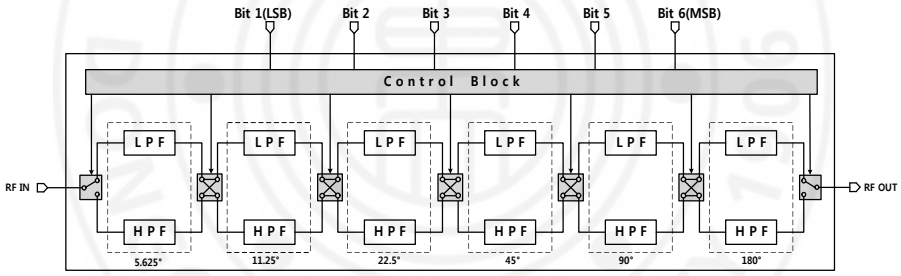


Figure 2.1-6 Block diagram of the proposed phase shifter

Figure 2.1-6 shows the block diagram of the proposed phase shifter using in this work. The phase shifter consists of 2 SPDT switches, 5 DPDT, phase shifting cells with LPF and HPF networks, and a bit controller. There are 6 bits to control the states of switches determining how much the phase of RF signals is shifted. The phase shifter covers the range of 360 degrees with the LSB of 5.625 degrees. The optimization can be applied to HP/LP filter networks and SPDT, DPDT control switches separately.

2.2 6-bits Digitally Attenuator

Six-bit CMOS digital attenuator is designed with resistive pi-type structure. The attenuator covers the range of 0 to 31.5 dB with the step of 0.5dB. Relative attenuation level is obtained by taking the difference between attenuation state and through the state which is controlled by single NMOS switches. One of the challenges in designing an attenuator is to achieve good enough impedance matching with characteristic impedance at both attenuation state and through the state.

There are two basic topologies mostly employed in the design of digital attenuator which is resistive Pi-type attenuator and resistive T-type attenuator. These conventional structures consist of series/shunt switch and resistors. The switches are usually realized by a single NMOS. Thus, NMOS transistors are key elements determining the performance of the digital step attenuator. For better understand, NMOS switches can be approximately modeled by the resistor R_{ON} in ON state and the capacitor C_{OFF} in OFF state. By neglecting body parasitic capacitance and series parasitic inductance, the schematic and equivalent circuits of attenuation state and reference state are shown in Figure 2.2-1 respectively.

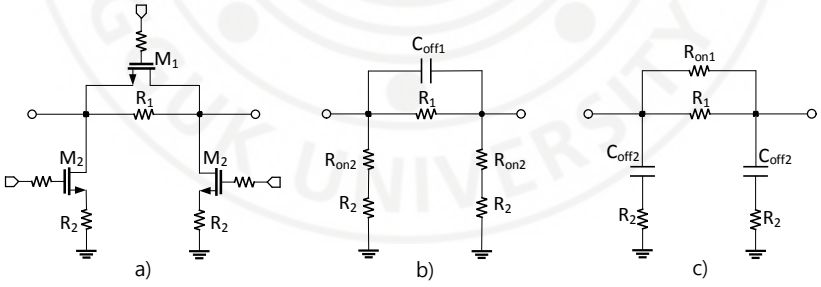


Figure 2.2-1 Schematic of Pi-type attenuator unit a) and simplified models in ON(b)/OFF(c) states.

2.3 Bidirectional gain amplifier (BDGA)

In the design of T/R chipset, there are several functional blocks such as phase shifter and attenuator. These blocks employ the switches as main elements to control the proper operation. Due to the high insertion loss caused by the conductive silicon substrate, the total insertion loss of the system is dominated by the loss of CMOS switches. As a result, there is an increasing demand for the wideband gain amplifier which will compensate for the loss of passive control circuit. The basic configuration of a microwave distributed amplifier is illustrated in Figure 2.3-1 .

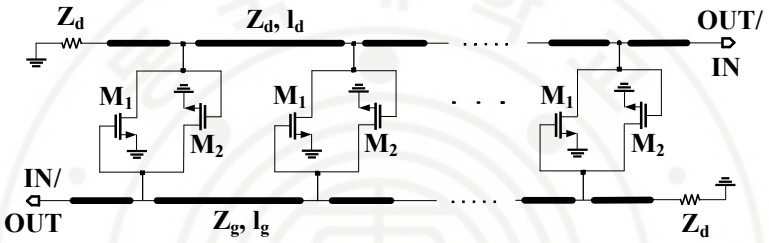


Figure 2.3-1 The configuration of an N-stage distributed amplifier.

It consists of N identical MOSFET cascaded, in which their gates and drains are connected to transmission lines having a characteristic impedance Z_g, Z_d and spacing of l_g, l_d respectively. To perform the amplifying operation, the gate line transmits the input signal to the gate terminal of each MOSFET, which will tap some of the input power. The output signals amplified by MOSFET form the travelling wave on the drain line. The gain of the amplifier is maximized by constructively adding of the output signals which implies that the phase delay of gate and drain lines must be matched. At the other ends of input and output lines, the termination impedances Z_g and Z_d absorb the signal propagating in the reverse direction. For current advanced CMOS process, typically, the routing interconnections have lengths of a few hundreds of microns; therefore, they cannot be used as transmission lines at frequency below 30 GHz. As a result, in monolithic integrated distributed

amplifier, the artificial transmission lines built by reactive lumped- element in ladder form are utilized. Figure 2.3-2 demonstrates for this configuration.

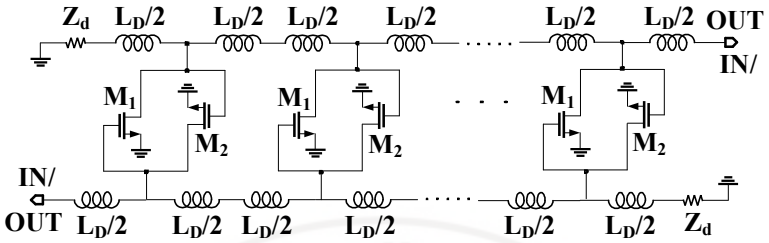


Figure 2.3-2 The schematic of a distributed amplifier with lumped-elements.

In this structure, the gate and drain capacitances of active devices play a part of artificial transmission line whilst the presence of the gate and drain resistances lead to the loss on these lines. At the other ends of input and output lines, the termination impedances absorb the signal propagating in the reverse direction and then prevent the input and output signals from the disturbance of signal reflection. In general, with the assumption that the transmission lines are lossless, the voltage gain of the conventional distributed amplifier can be expressed as below equation:

$$G = \frac{g_m Z_0 N}{2} \qquad (2.3\text{-}1)$$

Where N is the number of the distributed stages, g_m represents the transconductance of the single stage. Termination impedance Z_0 is typically $50\ \Omega$. It's worth noting that the factor of $\frac{1}{2}$ implies that half of the output signal travel along the opposite direction towards the drain termination. As observed from the gain equation, the conventional distributed amplifier shows the additive gain mechanism $N \times G_0$ contrasting with the gain of a cascade of N amplifier stages which increase as G_0^N. This fundamental characteristic of the conventional structure of distributed amplifier leads to the gain limitation, which is typically less than 10 dB for the presented designs.

Chapter 3 THE T/R MODULE WITH CONVENTIONAL BDGA

3.1 The system configuration of the T/R module in Design 1

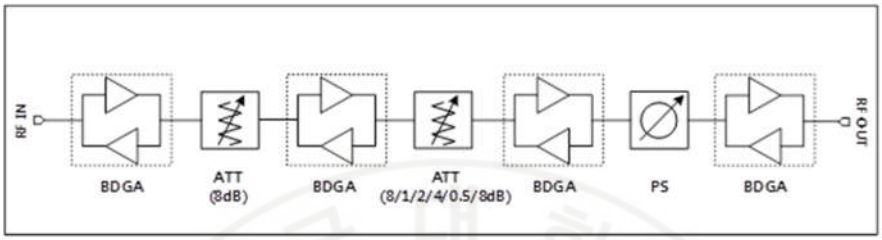


Figure 3.1-1 Block diagram of the T/R module in the first design.

Figure 3.1-1 illustrates the first design of T/R modules. The structure consists of a phase shifter block, a bit-control attenuator and BDGAs. The phase shifter is placed between two BDGAs to achieve better input and output return loss, resulting in a reduction of phase and amplitude variation in all phase shift states. Attenuator block is made up of several attenuation unit cells which are interspersed with BDGA blocks to diminish loading effect which causes an unusual step in attenuation states. There are 4 BDGAs employed in the structures to compensate the certain insertion loss of attenuator and phase shifter blocks and in addition, give specific gain for the whole chain. Three of them is comprised of 6 stages while the last one just has 2 stages. Detailed discussion about the first design is provided below.

3.2 The design of the 6-bit phase shifter

3.2.1 Phase shifting elements

Firstly, designing and optimizing for phase shift elements are performed. There are 2 types of HP/LP filter networks including T-type and Pi-type. Note that because a high-pass filter provides a leading phase while a low-pass filter provides a lagging phase, if each path contributes a half of the desired phase shift the phase difference

between two is fully the expected phase shift. Figure 2.1-6 describes the simplified circuit schematics of different type of HP/LP filter networks. Figure 3.2-1 shows the structures of passive filters used in phase shift sections. Equations are showing relations between the desired phase shift and values of L, C elements are summarized in Table 3.2-1. From these equations, device parameters for high-pass filter and a low-pass filter in Pi or T type are calculated in Table 3.2-2 below (Refer to Appendix for the detailed derivation of equations).

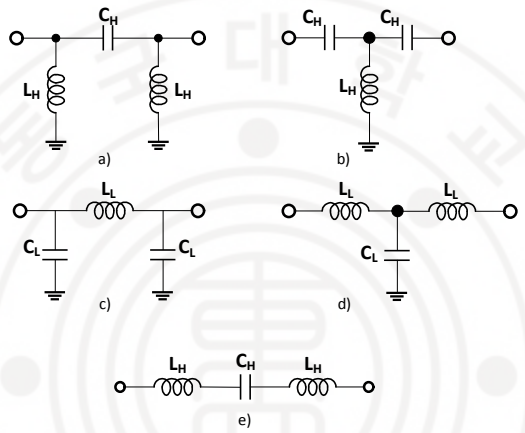


Figure 3.2-1 Third order filter networks used in the phase shifter.

Table 3.2-1 Design equations of L, C elements in LP/HP networks.

Filter		L	C
HP	T-type	$L=\frac{Z_0}{\omega\sin(\Delta\phi/2)}$	$C=\frac{1}{\omega Z_0\tan(\Delta\phi/4)}$
	π-type	$L=\frac{Z_0}{\omega\tan(\Delta\phi/4)}$	$C=\frac{1}{Z_0\omega\sin(\Delta\phi/2)}$
LP	T-type	$L=-\frac{Z_0}{\omega}\tan(\Delta\phi/4)$	$C=-\frac{\sin(\Delta\phi/2)}{\omega Z_0}$
	π-type	$L=-\frac{Z_0\sin(\Delta\phi/2)}{\omega}$	$C=-\frac{\tan(\Delta\phi/4)}{\omega Z_0}$

Table 3.2-2 Values of L, C elements corresponding to phase shift unit cells.

		ϕ(deg)	5.625	11.25	22.5	45	90	180
		ϕ (rad)	**0.098**	**0.196**	**0.393**	**0.785**	**1.571**	**3.142**
	HIGHPASS	**L-HP-T**	16.218	8.119	4.079	2.079	1.125	0.796
		C-HP-T	12.967	6.479	3.232	1.600	0.768	0.318
		L-HP- π	32.416	16.198	8.080	4.001	1.921	0.796
		C-HP-π	6.487	3.247	1.632	0.832	0.450	0.318
L	LOWPASS	**L-LP-T**	0.020	0.039	0.078	0.158	0.330	0.796
nH		**C-LP-T**	0.016	0.031	0.062	0.122	0.225	0.318
C		**L-LP-π**	0.039	0.078	0.155	0.305	0.563	0.796
pF		**C-LP-π**	0.008	0.016	0.031	0.063	0.132	0.318

Because of the limited range of inductance of on-chip inductors, as we can see on the above table, the high-pass filter network of phase shift blocks 11.25, 22.5 and 45 degree requiring excessive large inductances which cannot be implemented practically. Another approach is to use bandpass filter structure for leading phase branches of those phase shift units.

$$L = \frac{1 - \tan\phi_{21}.2Z_0\omega C}{2C\omega^2} \qquad (3.2\text{-}1)$$

Equation 3.2-1 shows the relation between the values of L, C elements with phase characteristic of the transfer function. Based on the above equation, inductance and capacitance of L, C elements can be obtained correspondingly. The device parameters are shown in Table 3.2-3.

Table 3.2-3 Element values used in phase units of 11.25, 22.5 and 45 degrees.

	11.25°	**22.5°**	**45°**
ϕ (°)	6.75	13.5	27
ϕ (rad)	0.117	0.235	0.471
C(fF)	1000.0	650.0	300.0
L(pH)	79.7	100.7	231.1

The summary of real values of the devices using in the phase shifter design is provided by Table 3.2-4.

Table 3.2-4 The real values of L, C elements used in the design of phase shifter.

Unit Cell	HP Filter		LP Filter	
	L (pH)	C (fF)	L (pH)	C (fF)
11.25°	80	1000	55	53
22.5°	101	624	110	86
45°	231	336	224	168
90°	1125	790	330	228
180°	796	272	796	336

The phase shifting cells are iteratively designed to achieve precise phase shift levels through fine tuning the values of inductors and capacitors. To save the chip area, spiral inductors are implemented on a top metal layer of aluminum whereas metal insulator metal (MIM) capacitors from the process design kit (PDK) are employed. All phase shift units are designed with passive structures simulated in the full-wave electromagnetic (EM) simulator HFSS, as illustrated in Figure 3.2-2 for 11.25° and 22.5° phase shift units.

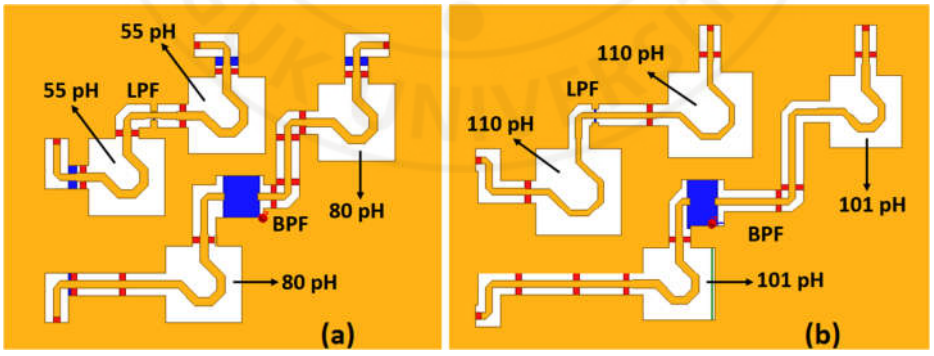


Figure 3.2-2 Passive parts of 11.25° (a) and 22.5° (b) cells used in HFSS.

3.2.2 The design of SPDT and DPDT switches.

To perform the phase shifting function with the coverage of 360° and the step of 5.625°, the switching mechanism is required. Switches enable to configure the path through phase shifting elements to produce the desired phase shifting level. This phase shifter employs 2 SPDT (single pole double throw) and 4 DPDT (double pole double throw) which circuit schematics are depicted in Figure 3.2-3 a) and b). For SPDT (the left figure), series transistors M_1, M_2 perform the main switching function. Shunt transistors M_3, M_4 are added with the purpose of improving the isolation between different paths.

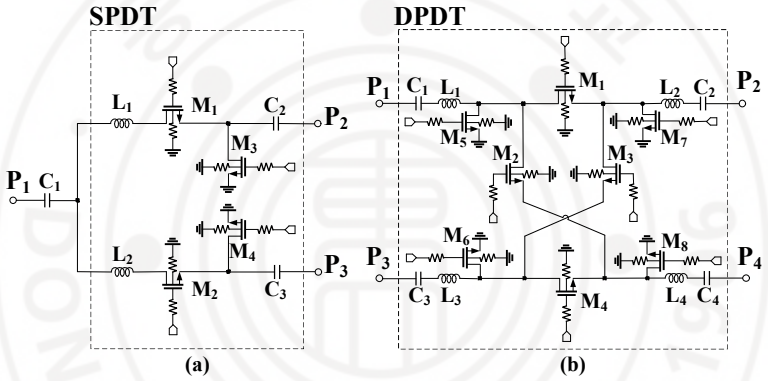


Figure 3.2-3 Circuit schematics of SPDT (a) and DPDT (b) switches.

In the design of SPDT and DPDT, the gate terminals are biased through a large resistor R_G to reduce fluctuations of V_{GD} and V_{GS} of transistors due to voltage swings at drain and source. This will keep the on resistance of transistors unchanged and avoid excessive voltage across the gate dielectric which causes breakdown issue. Because of the conductive silicon substrate of MOSFET devices, SPDT and DPDT switches show a relatively high insertion loss. To alleviate this effect, double -well body floating technique was applied. This technique also enhances the power handling capability of the circuit. Taking advantage of the triple-well CMOS process, the resistive body floating technique can be implemented simply by adding a large

resistor to bias the bulk. For the same purpose of resistive gate bias, through the large resistor, the bulk becomes RF floating that means its voltage will be bootstrapped to the source and drain voltage. The triple-well process proves the advantages in terms of noise, isolation and bulk control. Figure 3.2-4 shows the simplified cross-sectional view of an NMOS transistor in triple-well CMOS technology.

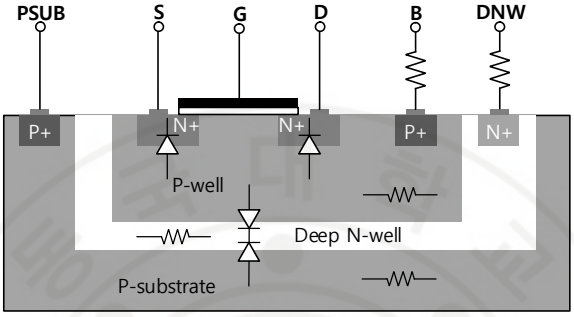


Figure 3.2-4 Illustration of double body floating technique.

The regional p-well and global p-substrate are isolated by the deep n-well layer introducing two other diodes: the diode formed by P-well and deep N-well, and the diode formed by deep N-well and P-substrate. A strong input signal can make source-body and/or drain-body diodes turn-on unintentionally, which cause linearity degradation. To prevent this phenomenon, the body of the MOSFET device should be floated at RF. By doing this, the body voltage is bootstrapped to the voltage swing of the input signal. Body floating technique can be easily realized by biasing body P-well through a large resistor. Making P-well floated at RF leads to another unintentional turn-on the phenomenon with the diode formed by P-well and deep N-well layer. Thus, the deep N-well should also be biased via a large resistor to make it floated.

Table 3.2-5 The device parameters used in SPDT and DPDT switches.

Device	**SPDT**	**Device**	**DPDT**
$\boldsymbol{M_1}$, $\boldsymbol{M_2}$	130 u/0.06 u (nf = 26, m = 2)	M_1~M_4	130 u/0.06 u (nf = 26, m = 2)
$\boldsymbol{M_3}$, $\boldsymbol{M_4}$	20 u/0.06 u (nf = 20)	M_5~M_8	20 u/0.06 u (nf = 20)
$\boldsymbol{L_1}$, $\boldsymbol{L_2}$	610 pH	L_1~L_4	510 pH
$\boldsymbol{C_1}$~$\boldsymbol{C_3}$	3.2 pF	C_1~C_4	3.2 pF

Table 3.2-5 lists all values of the devices utilized in SPDT and DPDT switches. All the passive parts in the SPDT/DPDT switches were simulated in HFSS simulator to examine the coupling effects of each inductor, as presented in Figure 3.2-5 a) and b).

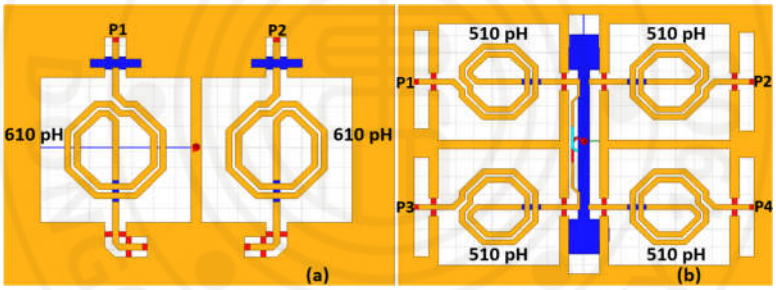


Figure 3.2-5 Passive parts of SPDT (a) and DPDT (b) switches used in HFSS.

The performance of SPDT and DPDT switches is examined by standalone simulation and summarized in Table 3.2-6 and Table 3.2-7 respectively.

Table 3.2-6 Performance parameters of SPDT switch in phase shifter design

Parameters	Frequency		
	8GHz	10GHz	12GHz
S_{21}	-1.59	-1.86	-2.32
S_{11}	-13.96	-14.6	-14.35
S_{22}	-17.75	-22.78	-33.81
S_{31}	-27.6	-24.96	-22.33
IP_{1dB}	12.85	11.51	9.55
OP_{1dB}	10.26	8.61	6.23

At 10 GHz, insertion losses of SPDT and DPDT are around 1.9 dB and 2.5 dB respectively. Input and output return loss is higher than 12 dB over the range of frequency from 8 GHz to 12 GHz.

Table 3.2-7 Performance parameters of DPDT switches in phase shifter design.

Parameters	Frequency		
	8GHz	10GHz	12GHz
S_{21}	-2.18	-2.49	-2.93
S_{11}	-14.59	-14.07	-12.48
S_{22}	-14.68	-14.17	-12.55
S_{31}	-29.25	-27.56	-26.37
S_{41}	-28.56	-26.95	-25.83
IP_{1dB}	13.79	13.46	13.25
OP_{1dB}	10.61	9.97	9.31

Because a DPDT (double pole double throw) switch has four different signal paths, we need 2 bits to control each switch. These control signals generate gate control voltages which will be applied to corresponding series and shunt transistors. Table 3.2-8 is the truth table for each case of the signal going through DPDT switches.

Table 3.2-8 Truth table of DPDT switch in the design of phase shifter.

	Input Bits	**Series switch controls**				**Shunt switch controls**			
Path	**C_1C_2**	**a_1**	**a_2**	**a_3**	**a_4**	**b_1**	**b_2**	**b_3**	**b_4**
P_1 to P_2	00	1	0	0	0	0	0	1	1
P_1 to P_4	01	0	0	1	0	0	1	1	0
P_3 to P_4	11	0	0	0	1	1	1	0	0
P_3 to P_2	10	0	1	0	0	1	0	0	1

The logic combination for generating transistor's gate voltage can be easily obtained based on the above truth table of a DPDT switch and shown in Table 3.2-9

Table 3.2-9 Logic combinations for control voltages in DPDT switches.

a_1	**a_2**	**a_3**	**a_4**
$\overline{C_1}\,\overline{C_2}$	$C_1\overline{C_2}$	$\overline{C_1}C_2$	C_1C_2
b_1	**b_2**	**b_3**	**b_4**
C_1	C_2	$\overline{C_1}$	$\overline{C_2}$

Finally, the proposed 6-bit phase shifter covers the full range of 360 degrees with the step size of 5.625 degrees. There are 64 phase shifting states, so it requires 6 bits to properly control the operation. Again, we need to create the truth table in which the input bits and expected output bits (to control the switches) are declared accordingly. Being noticed that LSB phase shifting unit and SPDT switches need a single bit while DPDT switches need a couple of bits for the control purpose. For the detailed description of the truth table, one can refer to the attached excel file. The results of the logic combination are shown in Table 3.2-10.

Table 3.2-10 Logic combination of control signals for DPDT switches.

CTL_1	**CTL_2**	**CTL_31**	**CTL_32**
$\mathbf{B_0}$	B_1	$\overline{B_1}$	$\overline{B_2}$
CTL_41	**CTL_42**	**CTL_51**	**CTL_52**
$\overline{\mathbf{B_2}}$	$\overline{B_3}$	$\overline{B_3}$	$\overline{B_4}$
CTL_61	**CTL_62**	**CTL_7**	**NA**
$\overline{\mathbf{B_4}}$	$\overline{B_5}$	B_5	NA

After designing at schematic level, laying out the circuit with real devices is performed. To make efficient use of chip area, the phase shift chain is laid out as captured in Figure 3.2-6.

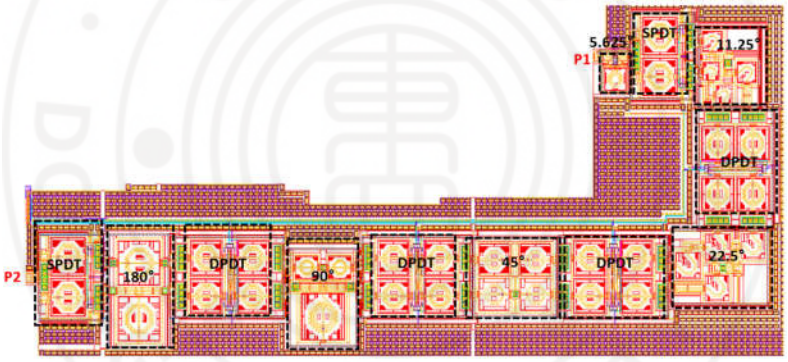


Figure 3.2-6 The full layout of the phase shifter in Design 1.

After extracting parasitic and running the post-layout simulation, phase shift characteristics in major states are shown in Figure 3.2-7. As can be seen, each phase shift unit provides the proper phase as designed.

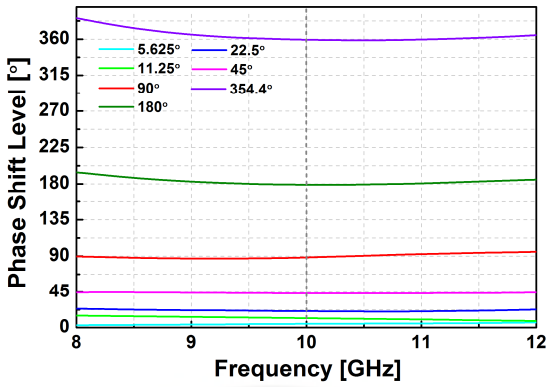


Figure 3.2-7 The post-layout simulation of the phase shifter in main phase states.

3.3 The design of attenuator

Figure 3.3-1 describes the proposed structure of digital controlled attenuator.

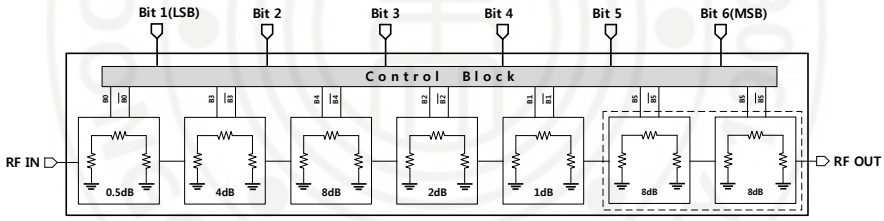


Figure 3.3-1 The block diagram of a 6-bit attenuator.

The detailed structure of a unit cell using in the attenuator design as shown in Figure 3.3-2. The pi-type attenuator is utilized in this design instead of T-type considering the range of resistance, which is possible to be fabricated in practical. To perform the switching function between attenuation state and through states, simple NMOS switches are used. Table 3.3-1 lists all the device parameters used in each attenuation unit cells.

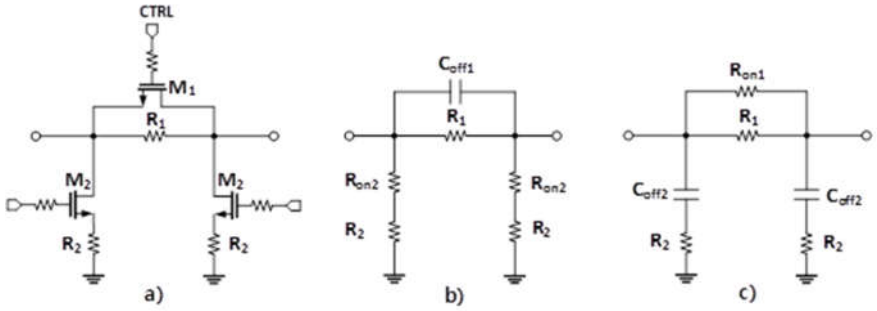


Figure 3.3-2 The schematic a) and ON b), OFF c) models of attenuation cell.

Table 3.3-1 Device parameters used in each attenuation unit cells.

Att. unit	M_1	M_2	R_1 (Ω)	R_2(Ω)
0.5 dB	40μ/0.06μ	4μ/0.06μ	6.7	9.12k
1 dB	40μ/0.06μ	4μ/0.06μ	15.2	3.04k
2 dB	40μ/0.06μ	4μ/0.06μ	21.7	372.4
4 dB	40μ/0.06μ	4μ/0.06μ	31.1	82.50
8 dB	40μ/0.06μ	4μ/0.06μ	78.5	33.5
8 dB (16)	40μ/0.06μ	4μ/0.06μ	81.3	33.5

Circuit layout has a significant impact on the performance of the RF integrated circuit. Thus, as captured in Figure 3.3-3, to avoid performance variation caused by layout parasitic, the attenuation chain is optimized in layout with signal paths formed by CPW.

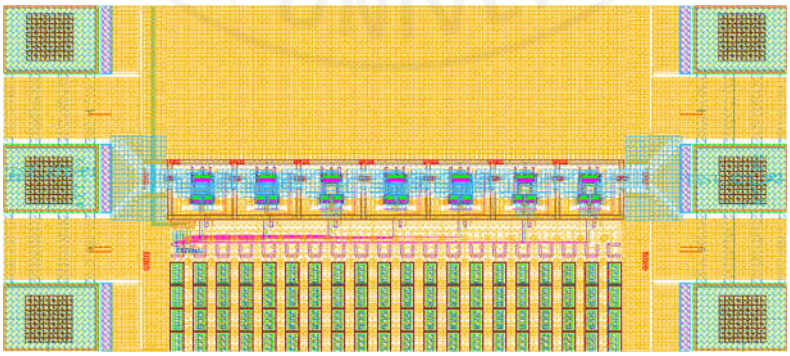


Figure 3.3-3 Circuit layout of the attenuator in Design 1.

After extracting parasitic and running the post-layout simulation, phase shift characteristic in major states are shown in Figure 3.3-4.

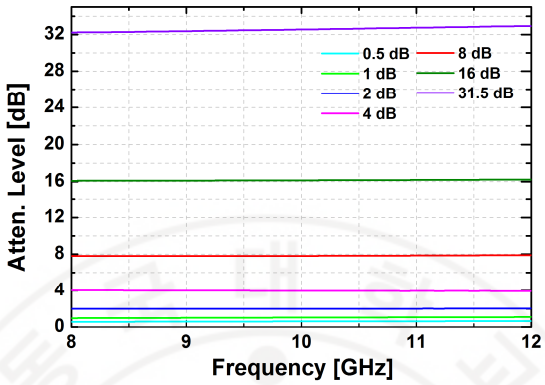


Figure 3.3-4 The simulated attenuation levels in main attenuation states.

3.4 The Bi-Directional Gain Amplifier (BDGA)

To provide the bidirectional operation for transmitting and receiving RF signals, each distributed stage is made up of two cascade transistor pair. Each branch takes responsibility for amplifying signals in forward and reverse mode respectively. Figure 3.4-1 shows the circuit schematic of the conventional BDGA.

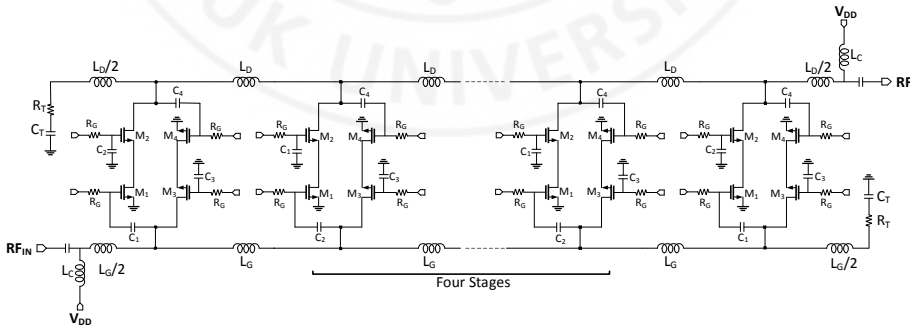


Figure 3.4-1 Circuit schematic of conventional BDGA with 6 stages of gain cell.

It consists of 6 stage cascode transistor pair (M_1 to M_4, gate and drain inductors (L_G and L_D), $50\ \Omega$ termination resistors, and RF choke inductors (L_C). Using cascode configuration provides some benefits such as better high-frequency response or high gain-bandwidth and simpler biasing. The mechanism to control the operational direction of the amplifier is set by activating one of the cascode transistor pair, which can be done by changing the bias voltages applying to gate terminals. For instance, in forward operation, transistor M_1 and M_2 are ON in saturation region and the transistor M_3 and M_4 are OFF. The shunt capacitances at the input are comprised of the gate capacitance of M_1 in saturation and drain capacitance of M_3 in off, which along with gate inductances $L_D/2$ form the artificial transmission line. By properly choosing MOSFET device sizes and inductor values, its characteristic impedance is approximately expressed as $Z_0 = \sqrt{\frac{L_G}{C_G}} = \sqrt{\frac{L_D}{C_D}}$ can achieve $50\ \Omega$. As a result, the circuit demonstrates wideband frequency response with better input and output return loss. To supply for the circuit in both operating modes, forward and backward, there are two VDD connecting at two ends of the amplifier. The capacitor at the gate of input transistor isolates its gate bias voltage from VDD. All bias voltages are provided through $30\ k\Omega$ resistors as shown in the figure.

The circuit layout of the BDGA captured in Figure 3.4-2 is optimized to be more compact to effectively reduce the effect of layout parasitic causing deteriorating on circuit performance.

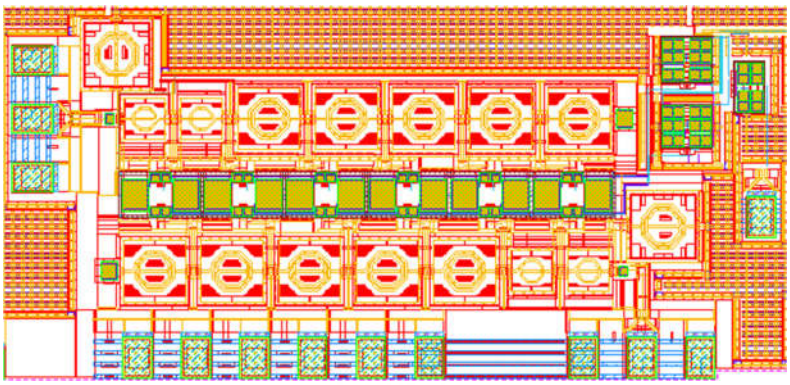


Figure 3.4-2 Circuit layout of the BDGA in Design 1.

After extracting parasitic and running the post-layout simulation, the main performance parameters of the BDGA circuit are shown in Figure 3.4-3 and Figure 3.4-4. For standalone simulation of BDGA in Design 1, as the nature of conventional BDGA structure whose gain is limited to be lower than 10 dB, simulated gain approximates to 9 dB at 10 GHz. The circuit also has Input and output return losses better than 10 dB, along with 5.7 dB of noise figure and over 60 dB of isolation coefficient. Regarding output/input power characteristic, depicts the output/input curve as well as 1 dB compression line. From the graph, it's observed that the BDGA block in Design 1 provides 4.95 dBm of OP1dB.

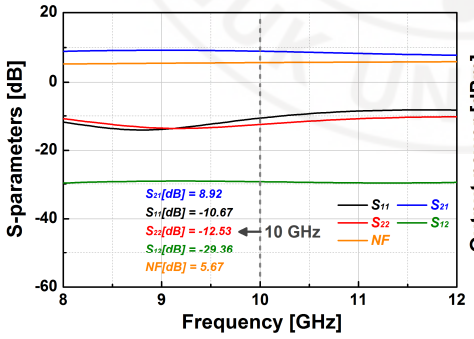


Figure 3.4-3 The Simulated S-parameters of the BDGA in Design 1.

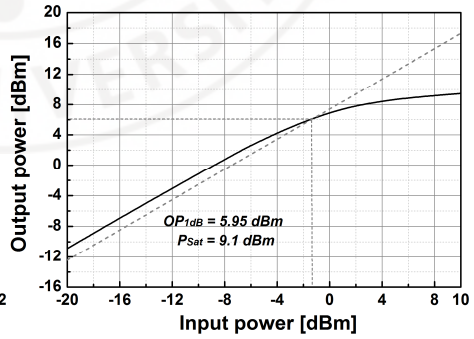


Figure 3.4-4 The simulated OP1dB of the BDGA in Design 1.

3.5 Full chip layout

The circuit layout of the whole chain of T/R modules in the first design as shown in Figure 3.5-1.

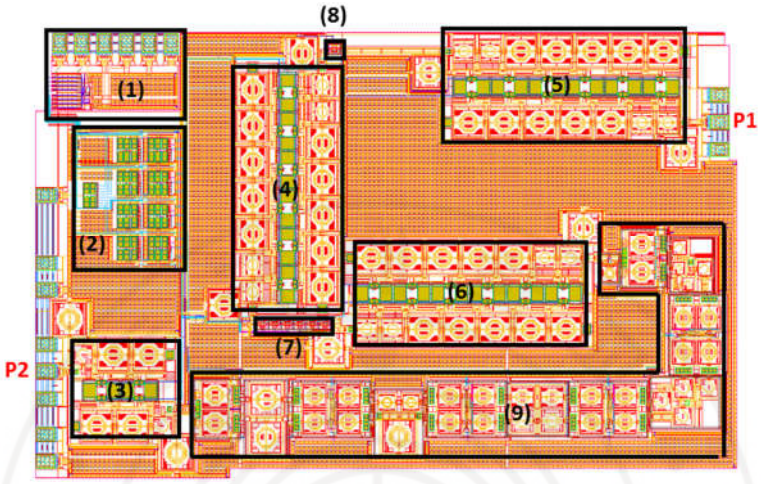


Figure 3.5-1 The full chip layout of the TRM in Design 1.

The system layout includes:

(1) SPI scan-chain	(4) 6-stage BDGA	(7) 5-bit Attenuator
(2) Bias block	(5) 6-stage BDGA	(8) 1-bit Attenuator
(3) 2-stage BDGA	(6) 6-stage BDGA	(9) 6-bit Phase Shifter

3.6 Measurement results of the T/R module in Design 1

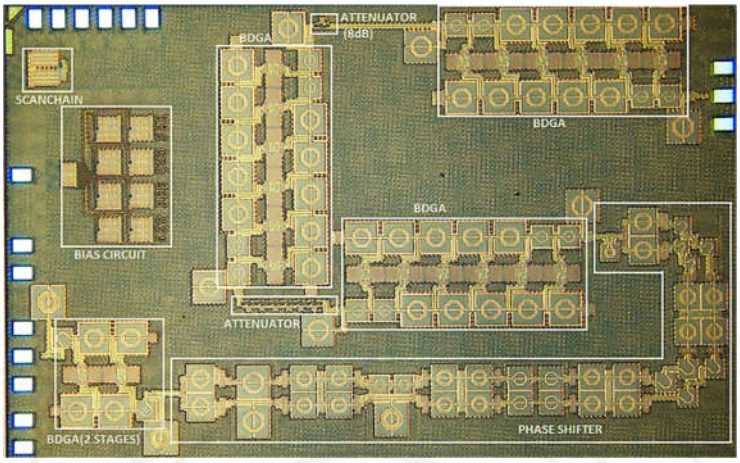


Figure 3.6-1 The microphotograph of the fabricated TRM in Design 1.

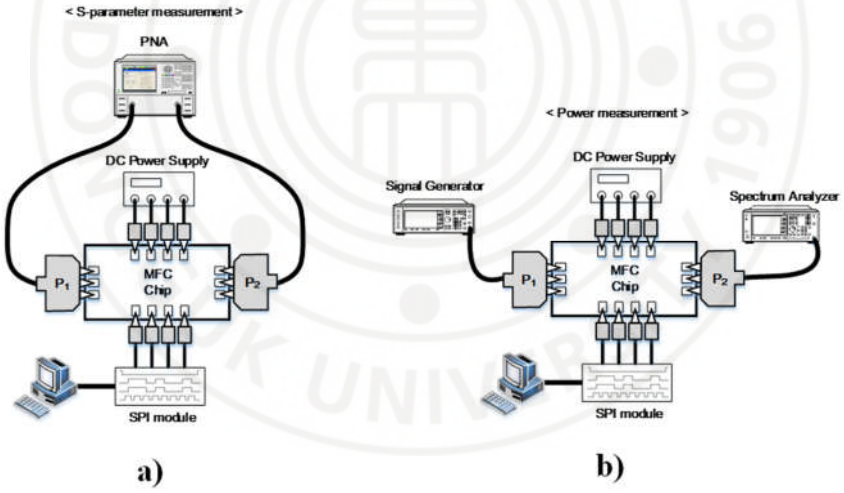


Figure 3.6-2 The block diagram of a) S-parameter and b) power measurement setup.

Figure 3.6-1 shows the microphotograph of the realized X-Band bi-directional T/R module fabricated in 65 nm CMOS process. The chip occupies an area of 3.92 × 2.44 mm^2 including pads. All the measurements were performed with on-chip

probing. Figure 3.6-2 a) and b) show the block diagram of the test facility in the measure of S-parameter and power respectively. In this setup, A 64-bit SPI scan-chain is used for controlling each block. The equipment used for measurement is as follows: Agilent E4407B spectrum analyzer, Keysight DSO-X 6002A digital oscilloscope, Keysight N5224A network analyzer, Agilent 83623B signal generator, and Agilent B2902A power supply. Figure 3.6-3 presents the measured S-parameters of the fabricated TRM at the reference state in which both phase shifter and attenuator blocks were set to zero. The transmission gain of the entire chain was around 3.8 dB at 10 GHz, which corresponds well with the simulation. The measured input (S_{11}) and output (S_{22}) return losses were higher than 10 dB, and the isolation (S_{12}) between Tx and Rx was better than 60 dB over the entire X-band. As depicted in Figure 3.6-4, the measured NF is about 10 dB at 10 GHz. The measured results of gain and output power of the fabricated TRM at different frequencies are shown in Figure 3.6-5. As can be seen, output P1dB was 5.13 dBm at 10 GHz satisfied the initial specification of the target application. The total DC current consumption was 142 mA with a 1.2 V supply voltage, which was mainly by the BDGAs. Figure 3.6-6 shows the measured result of the AM/PM conversion of the fabricated TRM at different frequencies. As can be seen from the graph, phase distortion is around 10° when input power approaches IP1dB.

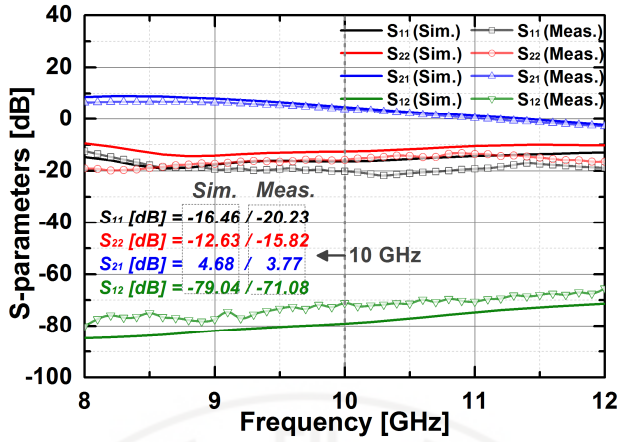


Figure 3.6-3 The measured S-parameters of the implemented TRM.

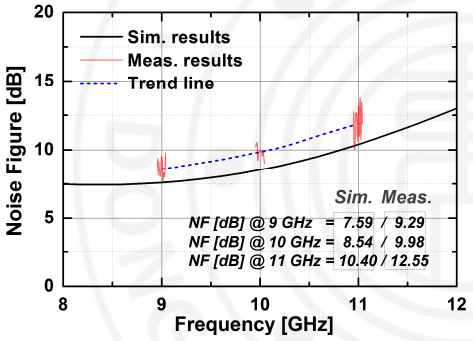


Figure 3.6-4 The measured noise figure of the implemented TRM.

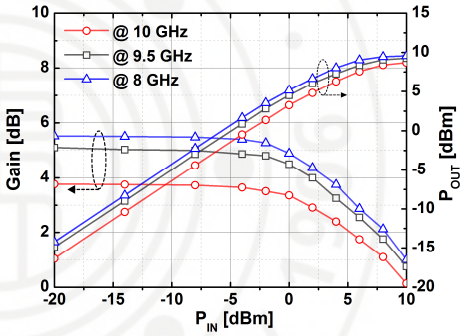


Figure 3.6-5 The measured gain and output power at different frequencies.

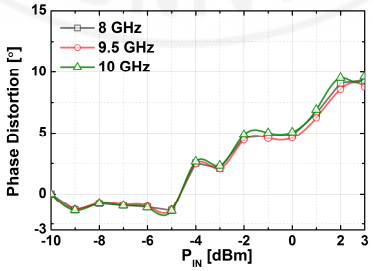


Figure 3.6-6 AM/PM conversions of the fabricated TRM at different frequencies.

Figure 3.6-7 shows the measured relative phase shift of the fabricated TRM in all 64 phase shift states. The system has capability to create a phase shift ranging from 0–360° with a minimum step of 5.625° at 8–12 GHz. Figure 3.6-8 demonstrates the correlation between the measured phase responses and the desired values at 10 GHz. To examine qualitatively the phase shifting performances of the implemented T/R module, the RMS values of phase and amplitude errors are provided. The RMS phase errors were lower than 4° from 9–11 GHz whereas the RMS amplitude error was smaller than 0.9 dB from 9–11 GHz, as depicted in Figure 3.6-9. Figure 3.6-11 presents the relative attenuation levels of the fabricated TRM in all 64 attenuation states after setting the phase shifter to default state. The system can provide an attenuation up to 31.5 dB with a minimum step of 0.5 dB at 8–12 GHz. Figure 3.6-12 presents a comparison between the measured amplitude levels and the expected values at 10 GHz. The RMS phase and amplitude errors in all the attenuation states at zero phase states are shown in Figure 3.6-10. From the graph, the measured RMS amplitude error was around 0.5 dB at 10 GHz while the RMS phase error was below 8° at 9-11 GHz. The phase errors over all phase shift states and attenuation errors over all attenuation levels at three different frequencies are presented in Figure 3.6-13 and Figure 3.6-14 respectively.

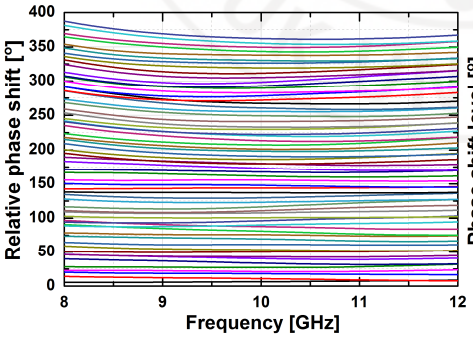


Figure 3.6-7 The relative phase shift levels of the fabricated TRM.

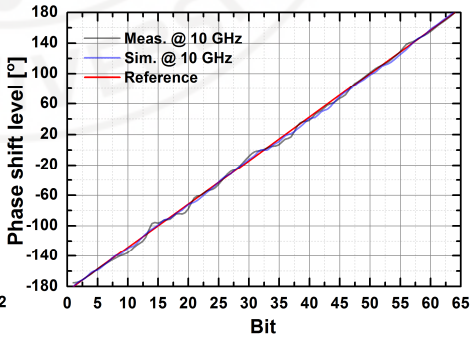


Figure 3.6-8 The measured phase shift levels vs. ideal values at 10 GHz.

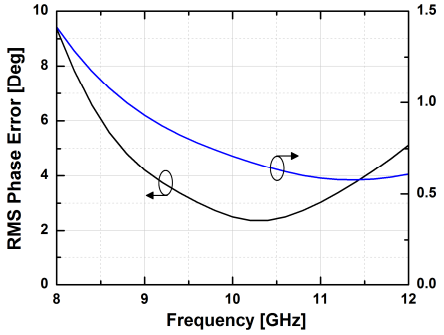


Figure 3.6-9 The RMS values of phase and amplitude errors vs. frequency.

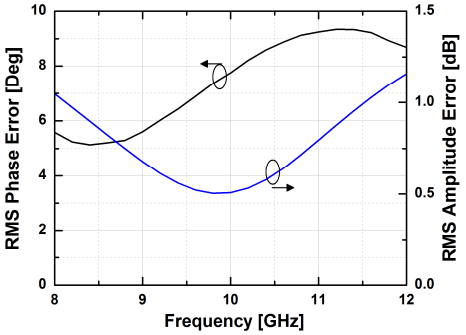


Figure 3.6-10 The RMS values of phase and amplitude errors vs. frequency.

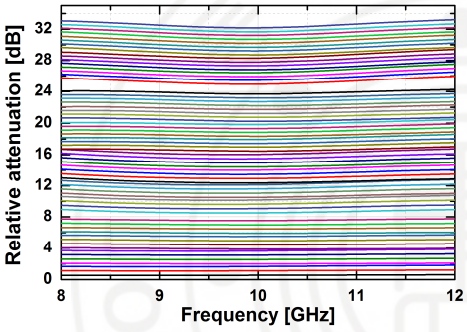


Figure 3.6-11 The relative attenuation levels of the TRM.

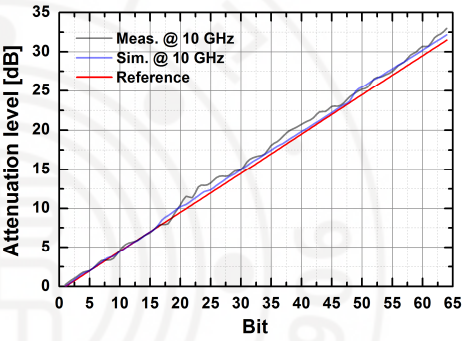


Figure 3.6-12 The measured attenuation levels vs. ideal values at 10 GHz.

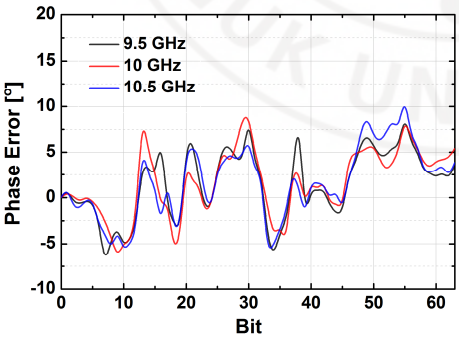


Figure 3.6-13 The phase errors of all phase states at different frequencies.

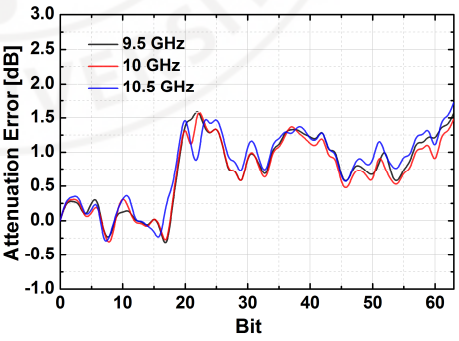


Figure 3.6-14 The atten. errors of all atten. states at different frequencies.

Table 3.2-1 provides the comparison of the measured performance of the implemented TRM with some published works in various device technologies. It demonstrates that the proposed TRM has the lowest power consumption with comparative performances.

Table 3.6-1 Performance comparison of TRMs for X-band phased array.

	[2]	**[14]**	**[18]**	**This work**
Technology	SiGe BiCMOS	SiGe BiCMOS	CMOS 0.18μm	CMOS 65nm
Frequency range (GHz)	8-11	8-11	8.5-10	8-10.5
Phase range/ step (deg)	360/11.25	360/11.25	360/5.625	360/5.625
Atten. range/ step (dB)	15.5/0.5	31/1	31.5/0.5	31.5/0.5
Insertion gain (dB)	17	20	12	3.7
RMS phase error (deg)	6	6	2	4
RMS amplitude error (dB)	1	1.5	0.25	0.5
Output P1dB (dBm)	12	18	11	5.1
NF	9	9	8.5	10
Power consumption (Watt)	0.8	1.5	0.67	0.17
Chip size (mm^2)	3.9×4.1	3.5×2.4	4.4×2.9	3.92 × 2.44

Chapter 4 THE T/R MODULE WITH THE CASCADED BDGA

4.1 System configuration

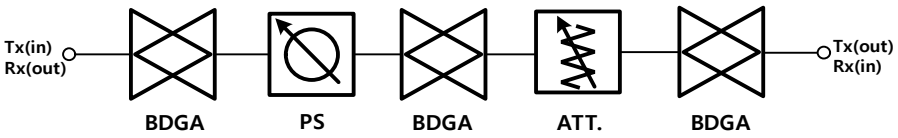


Figure 4.1-1 The configuration of the proposed TRM in design 2.

Figure 4.1-1 illustrates the second design of the T/R modules. The structure consists of a phase shifter block, a bit-control attenuator, and BDGAs. Similarly, the phase shifter is placed between two BDGAs to achieve better input and output return losses, resulting in a reduction of phase and amplitude variation in all phase shift states. Attenuator block is made up of several attenuation unit cells which are interspersed with BDGA blocks to diminish loading effect which causes an unusual step in attenuation states. There are just three BDGAs employed in Design 2 compared to Design 1. They are designed with a new structure which can provide better performance for the system as discussed below.

4.2 The new structure of BDGA

Conventional BDGA shows the limitation on gain due to not only the loss of artificial transmission lines but also the additive gain mechanism. To overcome this bottleneck, the cascaded BDGA shown in Figure 4.2-1 has been proposed.

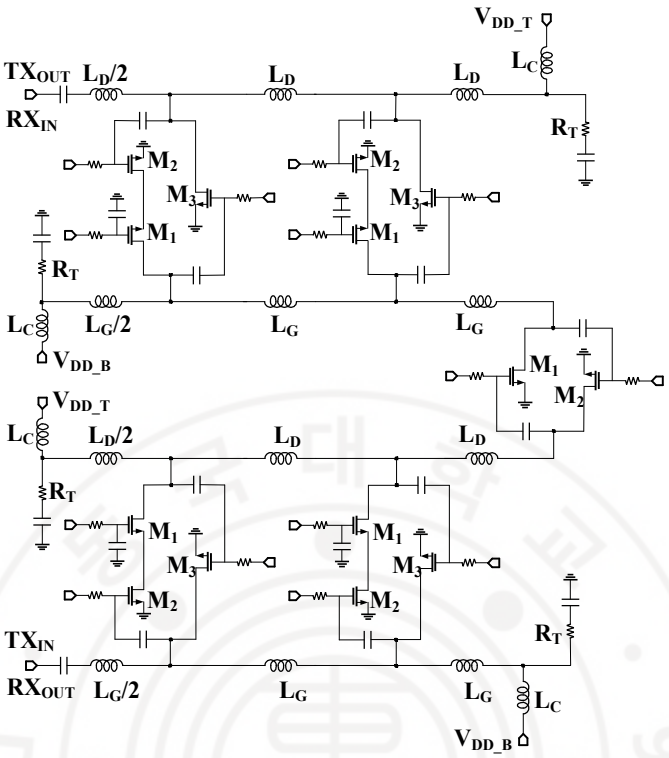


Figure 4.2-1 The schematic of proposed BDGA in Design 2.

The circuit is composed of two 2-stages BGAs at two ends and a gain-boosting stage at the middle. With the basic concept similarly to conventional BDGA, on-chip inductors and parasitic capacitances of transistors form the input and output artificial transmission lines which make the circuit broadband operation. Because of the cascade connection between three stages, the circuit takes advantage of the multiplicative gain mechanism. The voltage gain of cascaded BDGA can be expressed as:

$$A_V = A_{V1} \times A_{V2} \times A_{V3} = 2\left(g_{m1}\frac{Z_0}{2}\right) \times (g_{m2}Z_0) \times 2\left(g_{m3}\frac{Z_0}{2}\right) \qquad (4.2\text{-}1)$$

The number of gain cells in 1st stage and 3rd stage is chosen equal to 2 considering chip area which is comparable with existing conventional BDGAs. If the building elements of all three cascaded stages are made the same, even though the gain can

be significantly improved, the circuit will introduce output power limitation. Hence, the 1st stage employs a cascode transistor configuration which is better for gain production while 2nd and 3rd stages are made up by a single transistor in common source configuration demonstrating improvement on output power. The detailed structures of each cell are depicted in Figure 4.2-2 a) and b).

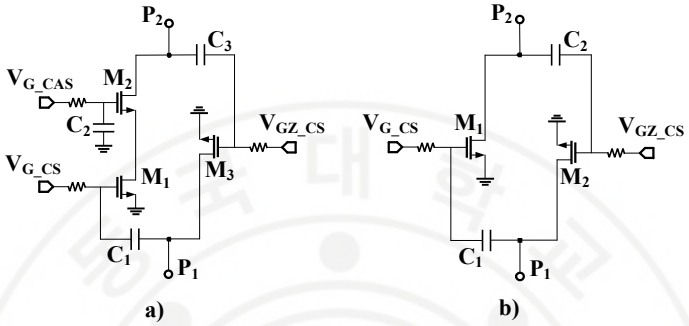


Figure 4.2-2 The circuit schematics of a) gain cell and b) gain boosting cell.

Value of the devices used in unit cells are shown in Table 4.2-1.

Table 4.2-1 Device parameters used in BDGA in Design 2.

2-end cells				Middle cell			
M_1	80µ/0.06µ	C_1	1.6pF	M_1	80µ/0.06µ	C_1	814fF
M_2	128µ/0.06µ	C_2	820fF	M_2	80µ/0.06µ	C_2	814fF
M_3	80µ/0.06µ	C_3	460fF				

The asymmetry of the unit gain cell does not affect the bidirectional function of the circuit. As can be seen in Figure 4.2-1, the forward and backward paths are totally identical. Figure 4.2-3 shows the microphotograph of the new structure BDGA. For standalone simulation of BDGA in Design 2, taking advantages of multiplicative gain mechanism compared to additive one in the previous version, new BDGA has such a high gain of more than 14 dB at 10 GHz as shown in Figure 4.2-4.

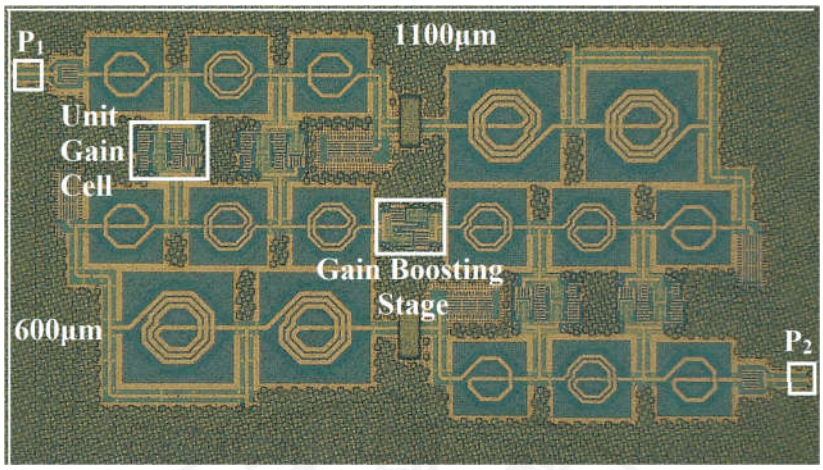


Figure 4.2-3 The microphotograph of the proposed BDGA in Design 2.

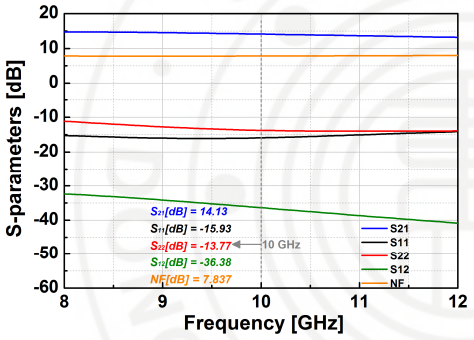


Figure 4.2-4 The simulated S-parameters of the BDGA in Design 2.

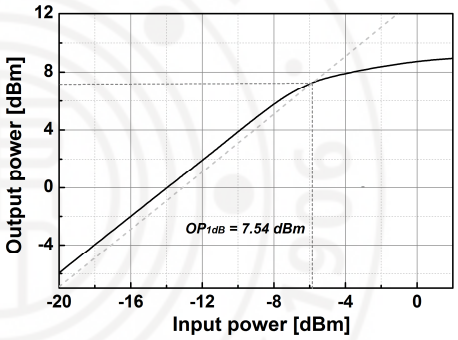


Figure 4.2-5 Input/output power characteristic of the BDGA in Design 2

The circuit also has input and output return loss better than 10 dB over the range of frequency from 8 to 12 GHz, along with 7.8 dB of noise figure and over 60 dB of isolation coefficient.

As mentioned in the previous section, the imbalanced structure of the BDGA unit cell with common source instead of cascode configuration at output stages can provide benefits in terms of output power level. Simulation results shown in Figure 4.2-5 can demonstrate for this observation. As can be seen from the graph, OP1dB achieves such a high value of 7.54 dBm at 10 GHz.

4.3 Full chip layout

The circuit layout of the whole chain of T/R modules in the first design as shown in Figure 4.3-1.

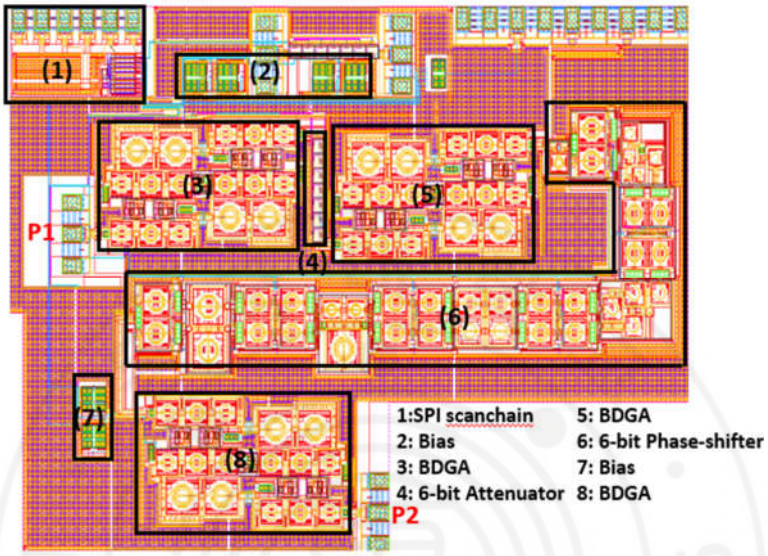


Figure 4.3-1 Full chip layout of the T/R modules in the second design.

Table 4.3-1 describes circuit improvements between TRM modules in Design 1 and Design 2.

Table 4.3-1 Comparison table between Design 1 and Design 2.

Block	Design 1	Design 2
BDGA	- Conventional structure with cascode configuration. - Low gain because of the additive gain mechanism. Low output P1dB due to the nature of cascode structure at the output.	- Enhanced structure with gain boosting stage at the middle cascading with 2 conventional BDGA taking advantage of the multiplicative gain mechanism. - Imbalanced unit cell to improve Output P1dB.

Phase Shifter		- Fine-tuning L, C elements to reduce phase errors.
Attenuator	- Single NMOS switches. - High amplitude error because of variation in NMOS operating condition. - Limitation in power handling capability.	- Single NMOS switches with a self-biasing mechanism - Reducing amplitude error and increasing power handling capability.

4.4 Simulation results of the whole chain of Design 2

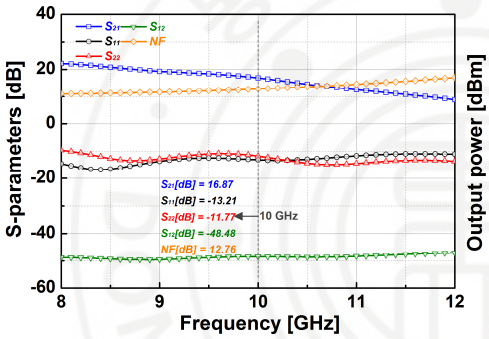


Figure 4.4-1 The simulated S-parameters of the TRM in Design 2.

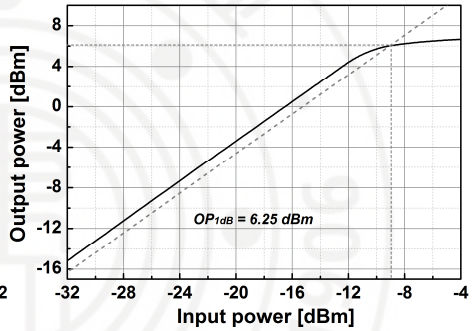


Figure 4.4-2 The simulated OP1dB of the TRM in Design 2

Post-layout simulations are performed with parasitic extraction netlist of the circuit, and the results are shown in Figure 4.4-1 . As can be seen, the system reaches higher than 16 dB of gain at 10 GHz as well as better than 10 dB of input/output return loss over a frequency range of X-band. Noise figure is about 12 dB at 10 GHz while isolation coefficient is higher than 60 dB from 8 to 12 GHz. These results prove the certain enhancement of Design 2 with respect to Design 1. Regarding input/output power characteristic of the entire T/R module in Design 2, as depicted in Figure 4.4-2, output P1dB of the system is 6.25 dBm at 10 GHz.

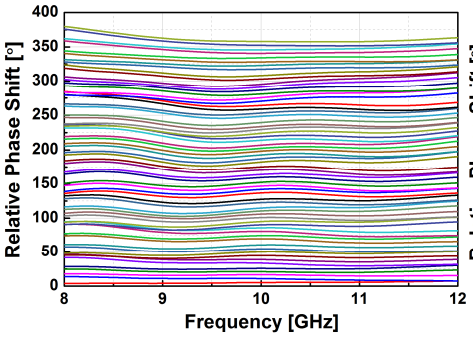


Figure 4.4-3 Simulated relative phase shift levels of the TRM in Design 2.

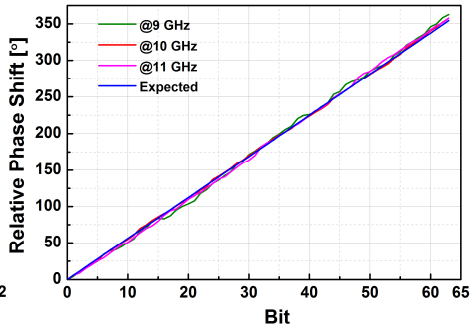


Figure 4.4-4 Simulated phase levels at 9 GHz, 10 GHz, and 11 GHz in Design 2.

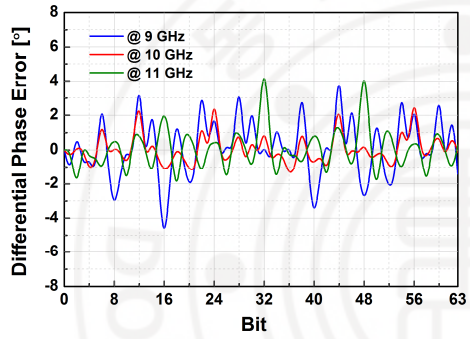


Figure 4.4-5 Simulated differential phase errors at 9-11 GHz in Design 2.

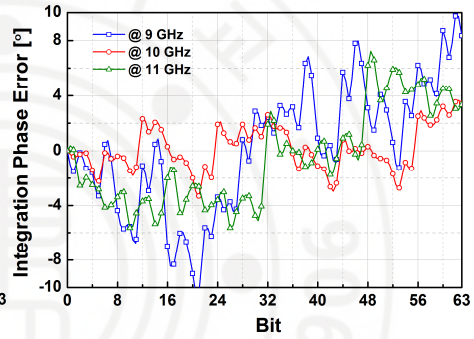


Figure 4.4-6 Simulated integrated phase errors at 9-11 GHz in Design 2.

Figure 4.4-3 shows the relative phase response of the T/R module in Design 2 in total 64 phase shift states. As can be seen, the system has the capability to generate a phase shift ranging from 0 to 360 degrees with a step of 5.625 degrees over a range of frequency from 8 to 12 GHz. Regarding phase shift error, Figure 4.4-4 demonstrates the correlation between the relative phase shift at some specific frequencies including 9 GHz, 10 GHz, and 11 GHz and the expected line.

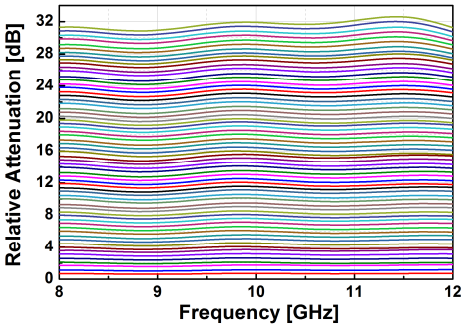


Figure 4.4-7 Simulated relative atten. levels of the TRM in Design 2.

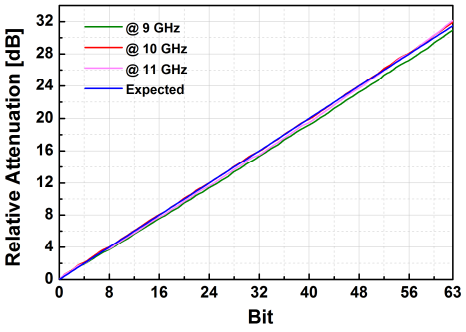


Figure 4.4-8 Simulated attenuation levels at 9, 10, and 11 GHz in Design 2.

More details about the errors are given in Figure 4.4-5 and Figure 4.4-6 which illustrate the differential and integration errors respectively. As can be seen from the graph, at 10 GHz, differential errors are below 3° while integration errors are less than 4° for all phase shift states. RMS phase and amplitude errors are also improved with respect to Design 1. It can be observed from RMS phase errors are less than 4° from 9.5 GHz to 11.5 GHz while RMS amplitude errors are below 0.75 dB from 9.5 GHz to 12 GHz.

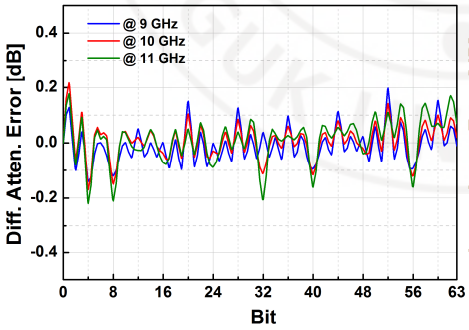


Figure 4.4-9 Simulated differential attenuation errors in Design 2.

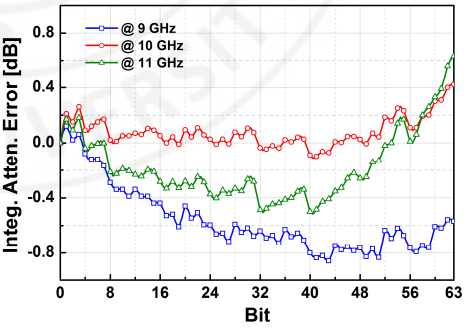


Figure 4.4-10 Simulated integral attenuation errors in Design 2.

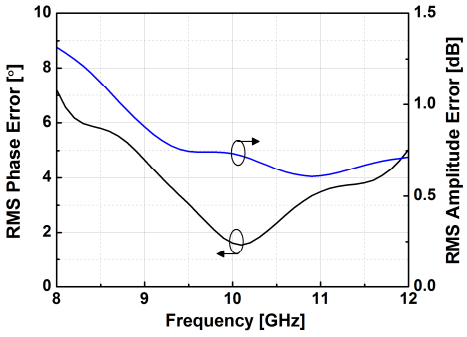


Figure 4.4-11 RMS phase/amplitude errors in 64 phase states of Design 2.

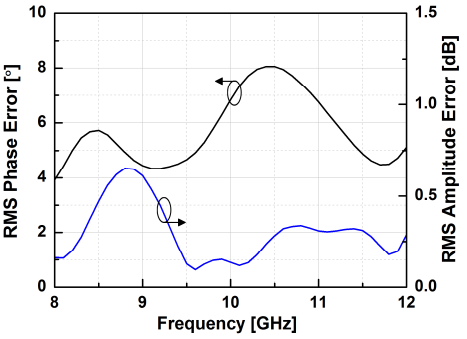


Figure 4.4-12 RMS phase/amplitude errors in 64 attenuation states of Design 2

Figure 4.4-7 depicts the total 64 states of relative attenuation when the phase shifter block is set in the reference state. The graph shows the better performance compared to the T/R module in Design 1. The distribution of 64 attenuation states is almost uniform over the range of frequency ranging from 8 GHz to 12 GHz. The enhancement in terms of attenuation error can also be observed from Figure 4.4-9 and Figure 4.4-10. Three lines in representing relative attenuation levels as 9 GHz, 10 GHz, and 11 GHz respectively as varying input control bits are well matched with the ideal line. Qualitatively, differential attenuation errors are below 0.2 dB in all states while integration errors are less than 0.5 dB in all states at 10 GHz. Finally, the RMS phase and amplitude errors in 64 attenuation states of the T/R module in Design 2 can be examined via Figure 4.4-11 and Figure 4.4-12. RMS amplitude errors are less than 0.5 dB from 9.5 GHz to 12 GHz while RMS phase errors are below 8° over the frequency range from 8 GHz to 12 GHz.

4.5 Performance comparison between Design 1 and Design 2

Table 4.5-1 describes the performance improvements of Design 2 with respect to Design 1.

Table 4.5-1 Performance comparison between Design 1 and Design 2.

		Design 1	Design 2
Gain [dB]		4.68	**16.87**
Input/Output return loss [dB]		16.46/12.63	13.21/11.77
NF [dB]		8.54	12.76
Output P1dB [dBm]		4.95	**6.25**
All Phase shift states	**Diff. Error**	$<4°$ @ 10 GHz	$<\mathbf{3}°$ @ 10 GHz
	Integ. Error	$<8°$ @ 10 GHz	$<\mathbf{4}°$ @ 10 GHz
	RMS phase error	$<4°$@ 9 -11.5 GHz	$<4°$ @ 9.5-11.5 GHz
	RMS amplitude error	$<0.75\ dB$ @ 10-12 GHz	$<0.75\ dB$ @ 9.5-12 GHz
All atten-uation states	**Diff. Error**	$<0.5\ dB$ @ 10 GHz	$<\mathbf{0.2}\ \boldsymbol{dB}$ @ 10 GHz
	Integ. Error	$<1\ dB$ @ 10 GHz	$<\mathbf{0.4}\ \boldsymbol{dB}$ @ 10 GHz
	RMS phase error	$<10°$ @ 8-12 GHz	$<\mathbf{8}°$ @ 8-12 GHz
	RMS amplitude error	$<0.75\ dB$ @ 9-11 GHz	$<\mathbf{0.7}\ \boldsymbol{dB}$ @ 8-12 GHz
DC current		142 mA	217.4 mA

Chapter 5 CONCLUSION

In this work, I proposed the structure of CMOS based T/R chipset with the phase coverage of $360°$ and the LSB of $5.625°$ and attenuation range of $31.5\ dB$ with a step size of $0.5\ dB$. Double-well floating technique was used to eliminate the loss caused many switched NMOS devices employed in SPDT and DPDT switches. The technique also improves the power handling capability of the circuit. Bi-directional gain amplifiers compensating the loss through the attenuator block with new structure provide adequate voltage gain and satisfy the requirement of output power for the entire system. New BDGA structure consists of two 2-stage conventional BDGA cascaded through the middle stage. By taking advantage of multiplicative gain mechanism compared to the additive gain mechanism, the proposed BDGA in this work provides higher than 10 dB of gain which is the limitation in the conventional design. In addition, the unit cell in the proposed BDGA is made imbalanced, which employs the simple common source structure at the output stage. This configuration can improve the output power of the amplifier up to 7.5 dBm even with 1.2 V of the supply voltage.

In the future, I plan to do more research to improve phase and attenuation errors. The power consumption of the entire system should also be decreased to meet the requirement of low power applications.

REFERENCES

[1] Visser, Hubregt J. (2006) *Array and Phased Array Antenna Basics*, John Wiley & Sons. pp. xi. ISBN 0470871180

[2] N. Carosi, A. Bettidi, A. Nanni, L. Marescialli, and A. Cetronio, "A mixed-signal X-band SiGe multi-function control MMIC for phased array radar applications," in *Proc. 39th Eur. Radar Conf., Oct. 2009, pp. 240-243.*

[3] Wikipedia. *Phased Array.* Available: http://en.wikipedia.org/wiki/Phased_array

[4] Wikipedia. *Karl Ferdinand Braun*. Available: https://en.wikipedia.org/wiki/Karl_Ferdinand_Braun.

[5] E. Brookner, "Phased-array radars," *Scientific American*, vol. 252, pp. 94-102, 1985.

[6] J. Wenger, "Automotive radar - status and perspectives," *IEEE Compound Semiconductor Integrated Circuit Symposium, 2005. CSIC '05.*, 2005, pp. 4.

[7] Wu, Liyong et al. "An RF Phased Array Applicator Designed for Hyperthermia Breast Cancer Treatments." *Physics in medicine and biology* 51.1 (2006).

[8] "AESA, other developments drive radar production," *Forecast International, 2008.*

[9] P. Schuh, H. Sledzik, R. Reber, K. Widmer, A. Fleckenstein, B. Schweizer, and M. Oppermann, "T/R module technologies today and future trends," in *Proc. 39th Eur. Microwave Conf., Oct. 2010, pp. 1540-1543.*

[10] E. Brookner, "Active-phased-arrays and digital beamforming: Amazing breakthroughs and future trends," *2008 IEEE Radar Conference*, Rome, 2008, pp. 1-2.

[11] "XZ1002-BD, 8.5–11.0 GHz GaAs MMIC Core Chip," M/A-COM Tech Asia. Available online: https://www.digchip.com/datasheets/3262797-8-5-11-0-ghz-gaas-mmic-core.html (accessed on 28 May 2018).

[12] Product Datasheet: CGY2170YUH: C Band High Gain Low Noise Amplifier. OMMIC: Limeil-Brévannes, France. Available online: www.ommic.fr/file/download/CGY2178UH_DS_130910.pdf (accessed on 8 May 2018).

[13] B. Min and G. M. Rebeiz, "A 10–50-GHz CMOS Distributed Step Attenuator with Low Loss and Low Phase Imbalance," in *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2547-2554, Nov. 2007.

[14] G. M. Rebeiz et al., "G. Highly dense microwave and millimeter wave phased array T/R modules using CMOS and SiGe RFICs," *2011 IEEE 12th Annual Wireless Microwave Technology Conference*, Clearwater Beach, FL, USA, April 2011, pp. 1-5.

[15] T. Dinc, S. Zihir, and Y. Gurbuz, "SiGe building blocks for on-chip X-Band T/R modules," *2012 IEEE 12th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Santa Clara, CA, 2012, pp. 57-60.

[16] J. C. Jeong and I. B. Yom, "X-band high power SiGe BiCMOS multi-function chip for active phased array radars," in *Electronics Letters*, vol. 47, no. 10, pp. 618 -619, 12 May 2011.

[17] C. E. Patterson et al., "A Lightweight Organic X-Band Active Receiving Phased Array with Integrated SiGe Amplifiers and Phase Shifters," in *IEEE Transactions on Antennas and Propagation*, vol. 59, no. 1, pp. 100-109, Jan. 2011.

[18] D. Kang, J. Kim, B. Min, and G. M. Rebeiz, "Single and Four-Element Ka-Band Transmit/Receive Phased-Array Silicon RFICs with 5-bit Amplitude

and Phase Control," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3534-3543, Dec. 2009.

[19] B. Ku, D. Kang and S. Hong, "CMOS integrated circuits for X-band phased array systems," *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Seoul, 2011, pp. 1-5.

[20] Moon-Kyu Cho, Seung-Hwan Yoon, Sanghoon Sim, L. Jeon, and Jeong-Geun Kim, "CMOS-based Bi-directional T/R chipsets for phased array antenna," *2012 IEEE/MTT-S International Microwave Symposium Digest*, Montreal, QC, 2012, pp. 1-3.

[21] J. Han, J. Kim, J. Park, and J. Kim, "A 28 GHz four channel T/R chipset in 65 nm CMOS technology," *2016 IEEE 5th Asia-Pacific Conference on Antennas and Propagation (APCAP)*, Kaohsiung, 2016, pp. 203-204.

[22] W. K. Lo, W. S. Chan, C. W. Li, and C. K. Leung, "Self-phase equalised bidirectional distributed amplifier," in *Electronics Letters*, vol. 43, no. 11, pp. 626-627, 24 May 2007.

[23] J. M. Yang et al., "Compact ka-band bi-directional amplifier for low-cost electronic scanning array antenna," in *IEEE Journal of Solid-State Circuits*, vol. 39, no. 10, pp. 1716-1719, Oct. 2004.

[24] B. Min and G. M. Rebeiz, "Ka-Band Low-Loss and High-Isolation Switch Design in 0.13-μCMOS," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 6, pp. 1364-1371, June 2008.

[25] T. Dinc, S. Zihir, and Y. Gurbuz, "CMOS SPDT T/R switch for X-band, on-chip radar applications," in *Electronics Letters*, vol. 46, no. 20, pp. 1382-1384, 30 September 2010.

[26] Feng-Jung Huang and K. O, "A 0.5μm CMOS T/R switch for 900-MHz wireless applications," in *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 486-492, March 2001.

[27] A. A. Kidwai, C. Fu, J. C. Jensen, and S. S. Taylor, "A Fully Integrated Ultra-Low Insertion Loss T/R Switch for 802.11b/g/n Application in 90 nm CMOS Process," in *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1352-1360, May 2009.

[28] Zhenbiao Li, Hyun Yoon, Feng-Jung Huang, and K. K. O, "5.8-GHz CMOS T/R switches with high and low substrate resistances in a 0.18-μm CMOS process," in *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 1, pp. 1-3, Jan. 2003.

[29] Mei-Chao Yeh, Zuo-Min Tsai, Ren-Chieh Liu, K. -. Lin, Ying-Tang Chang, and Huei Wang, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 1, pp. 31-39, Jan. 2006.

[30] Q. Li, Y. P. Zhang, K. S. Yeo and W. M. Lim, "16.6- and 28-GHz Fully Integrated CMOS RF Switches with Improved Body Floating," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 2, pp. 339-345, Feb. 2008.

[31] Nagra, A. S., & York, R. A., "Distributed analog phase shifters with low insertion loss," in *IEEE Transactions on Microwave Theory and Techniques*, 47(9), 1705-1711,1999.

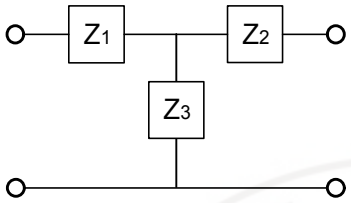
[32] Ellinger, F., Vogt, R., & Bachtold, W., "Compact reflective-type phase-shifter MMIC for C-band using a lumped-element coupler," in *IEEE Transactions on Microwave Theory and Techniques*, 49(5), 913-917.,2001

[33] Ellinger, F., Lott, U., & Bachtold, W., "An antenna diversity MMIC vector modulator for HIPERLAN with low power consumption and calibration capability," in *IEEE Transactions on Microwave Theory and Techniques*, 49(5), 964-969, 2001

APPENDIX

A. The equations for calculating L, C elements in third order filters

- **High-pass/Low-pass T-type topology**



$$A = 1 + \frac{Z_1}{Z_3} = 1 + Z_1 Y_3$$

$$B = Z_1 + Z_2 + \frac{Z_1 Z_2}{Z_3} = Z_1 + Z_2 + Z_1 Z_2 Y_3$$

$$C = Y_3$$

$$D = 1 + \frac{Z_2}{Z_3} = 1 + Z_2 Y_3$$

From ABCD to S-parameter conversion, we have:

$$S_{21} = \frac{2}{A + \frac{B}{Z_0} + CZ_0 + D} = \frac{2}{1 + Z_1 Y_3 + \frac{Z_1 + Z_2 + Z_1 Z_2 Y_3}{Z_0} + Y_3 Z_0 + 1 + Z_2 Y_3}$$

To substitute $z_1 = Z_1 / Z_0, z_2 = Z_2 / Z_0, y_3 = Y_3 Z_0$ we have:

$$S_{21} = \frac{2}{1 + z_1 y_3 + z_1 + z_2 + z_1 z_2 y_3 + y_3 + 1 + z_2 y_3}$$

$$S_{21} = \frac{2}{2 + z_1 + z_2 + y_3 (1 + z_1 + z_2 + z_1 z_2)}$$

$$S_{21} = \frac{2}{2 + 2jX_n + jB_n (1 + 2jX_n - X_n^2)} = \frac{2}{2(1 - X_n B_n) + j(2X_n + B_n - X_n^2 B_n)}$$

$$\tan\phi = -\frac{2X_n + B_n - X_n^2 B_n}{2(1 - X_n B_n)} \quad (1)$$

$$S_{11} = \frac{A + \frac{B}{Z_0} - CZ_0 - D}{A + \frac{B}{Z_0} + CZ_0 + D} = 0 \Rightarrow \frac{B}{Z_0} = CZ_0 \Rightarrow B = CZ_0^2 \Rightarrow Z_1 + Z_2 + Z_1 Z_2 Y_3 = Y_3 Z_0^2$$

To substitute $z_1 = Z_1 / Z_0, z_2 = Z_2 / Z_0, y_3 = Y_3 Z_0$ we have:

$$z_1+z_2+z_1z_2y_3=y_3 \Rightarrow y_3=\frac{z_1+z_2}{1-z_1z_2} \Rightarrow jB_n=\frac{2jX_n}{1-(jX_n)^2} \Rightarrow B_n=\frac{2X_n}{1+X_n^2} \quad (2)$$

To substitute (2) into (1) we have

$$\tan\phi=\frac{2X_n}{X_n^2-1} \Rightarrow (\tan\phi)X_n^2-2X_n-\tan\phi=0$$

High-pass T-network ($0 < \phi < 90°$)

$$jX_n=\frac{-j}{Z_0\omega C} \Rightarrow X_n=\frac{-1}{Z_0\omega C}<0$$

$$\Rightarrow X_n=\frac{1-\sqrt{1+\tan^2\phi}}{\tan\phi}=-\tan\left(\frac{\phi}{2}\right) \Rightarrow \frac{-1}{\omega CZ_0}=-\tan\left(\frac{\phi}{2}\right)$$

$$\Rightarrow C=\frac{1}{\omega Z_0\tan\left(\frac{\phi}{2}\right)}$$

$$jB_n=\frac{Z_0}{j\omega L} \Rightarrow B_n=-\frac{Z_0}{\omega L}<0$$

$$\Rightarrow B_n=\frac{2X_n}{1+X_n^2}=-\sin\phi \Rightarrow -\frac{Z_0}{L\omega}=-\sin\phi$$

$$\Rightarrow L=\frac{Z_0}{\omega\sin\phi}$$

Low-pass T-network ($-90° < \phi < 0$)

$$jX_n=\frac{j\omega L}{Z_0} \Rightarrow X_n=\frac{\omega L}{Z_0}>0$$

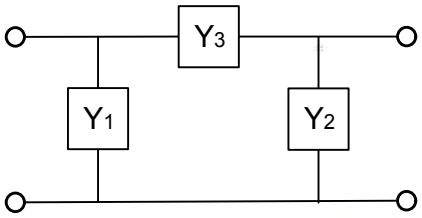
$$\Rightarrow X_n=\frac{1-\sqrt{1+\tan^2\phi}}{\tan\phi}=-\tan\left(\frac{\phi}{2}\right) \Rightarrow \frac{\omega L}{Z_0}=-\tan\left(\frac{\phi}{2}\right)$$

$$\Rightarrow L=-\frac{Z_0}{\omega}\tan\left(\frac{\phi}{2}\right)$$

$$jB_n=j\omega CZ_0 \Rightarrow B_n=\omega CZ_0$$

$$\Rightarrow B_n=\frac{2X_n}{1+X_n^2}=-\sin\phi \Rightarrow \omega CZ_0=-\sin\phi \Rightarrow C=-\frac{\sin\phi}{\omega Z_0}$$

- **High-pass/ Low-pass π-type topology**



$$A = 1 + \frac{Y_2}{Y_3} = 1 + Y_2 Z_3$$

$$B = \frac{1}{Y_3} = Z_3$$

$$C = Y_1 + Y_2 + \frac{Y_1 Y_2}{Y_3} = Y_1 + Y_2 + Y_1 Y_2 Z_3$$

$$D = 1 + \frac{Y_1}{Y_3} = 1 + Y_1 Z_3$$

From ABCD to S-parameter conversion, we have:

$$S_{21} = \frac{2}{A + \frac{B}{Z_0} + CZ_0 + D} = \frac{2}{1 + Y_2 Z_3 + \frac{Z_3}{Z_0} + (Y_1 + Y_2 + Y_1 Y_2 Z_3) Z_0 + 1 + Y_1 Z_3}$$

To substitute $y_1 = Y_1 Z_0, y_2 = Y_2 Z_0, z_3 = Z_3 / Z_0$ we have:

$$S_{21} = \frac{2}{1 + y_2 z_3 + z_3 + y_1 + y_2 + y_1 y_2 z_3 + 1 + y_1 z_3}$$

$$S_{21} = \frac{2}{2 + y_1 + y_2 + z_3 (1 + y_1 + y_2 + y_1 y_2)}$$

$$S_{21} = \frac{2}{2 + 2jB_n + jX_n (1 + 2jB_n - B_n^2)} = \frac{2}{2(1 - X_n B_n) + j(2B_n + X_n - B_n^2 X_n)}$$

$$\tan\phi = -\frac{2B_n + X_n - B_n^2 X_n}{2(1 - X_n B_n)} \quad (1)$$

$$S_{11} = \frac{A + \frac{B}{Z_0} - CZ_0 - D}{A + \frac{B}{Z_0} + CZ_0 + D} = 0 \Rightarrow \frac{B}{Z_0} = CZ_0 \Rightarrow B = CZ_0^2$$

$$\Rightarrow Z_3 = (Y_1 + Y_2 + Y_1 Y_2 Z_3) Z_0^2 \Rightarrow y_1 + y_2 + y_1 y_2 z_3 = z_3 \Rightarrow z_3 = \frac{y_1 + y_2}{1 - y_1 y_2}$$

$$\Rightarrow jX_n = \frac{2jB_n}{1 - (jB_n)^2} \Rightarrow X_n = \frac{2B_n}{1 + B_n^{\,2}} (2)$$

To substitute (2) into (1) we have:

$$\tan\phi = \frac{2B_n}{B_n^2 - 1} \Rightarrow (\tan\phi)B_n^2 - 2B_n - \tan\phi = 0$$

High-pass π-network ($0 < \phi < 90°$)

$$jB_n = \frac{Z_0}{j\omega L} \Rightarrow B_n = \frac{-Z_0}{\omega L} < 0$$

$$\Rightarrow B_n = \frac{1-\sqrt{1+\tan^2\phi}}{\tan\phi} = -\tan\left(\frac{\phi}{2}\right) \Rightarrow \frac{-Z_0}{\omega L} = -\tan\left(\frac{\phi}{2}\right) \Rightarrow L = \frac{Z_0}{\omega\tan\left(\frac{\phi}{2}\right)}$$

$$jX_n = \frac{1}{j\omega C Z_0} \Rightarrow X_n = -\frac{1}{\omega C Z_0} < 0$$

$$\Rightarrow X_n = \frac{2B_n}{1+B_n^2} = -\sin\phi \Rightarrow -\frac{1}{\omega C Z_0} = -\sin\phi \Rightarrow C = \frac{1}{Z_0\omega\sin\phi}$$

Low-pass π-network ($-90° < \phi < 0$)

$$jB_n = j\omega C Z_0 \Rightarrow B_n = \omega C Z_0 > 0$$

$$\Rightarrow B_n = \frac{1-\sqrt{1+\tan^2\phi}}{\tan\phi} = -\tan\left(\frac{\phi}{2}\right) \Rightarrow \omega C Z_0 = -\tan\left(\frac{\phi}{2}\right)$$

$$\Rightarrow C = -\frac{\tan\left(\frac{\phi}{2}\right)}{\omega Z_0}$$

$$jX_n = \frac{j\omega L}{Z_0} \Rightarrow X_n = \frac{\omega L}{Z_0} > 0$$

$$\Rightarrow X_n = \frac{2B_n}{1+B_n^2} = -\sin\phi \Rightarrow \frac{\omega L}{Z_0} = -\sin\phi \Rightarrow L = -\frac{Z_0\sin\phi}{\omega}$$

- **Bandpass filter topology**

ABCD matrix for the above structure is described as the below.

$$A = 1; B = Z_1 + Z_2 + Z_3; C = 0; D = 1$$

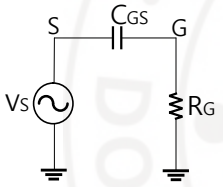
$$S_{21} = \frac{2}{A + \frac{B}{Z_0} + CZ_0 + D} = \frac{2}{2 + \frac{Z_1 + Z_2 + Z_3}{Z_0}}$$

$$= \frac{2}{2 + \frac{j2L\omega - \frac{j}{C\omega}}{Z_0}} = \frac{2}{2 + j\frac{2LC\omega^2 - 1}{Z_0\omega C}}$$

$$\Rightarrow \tan\phi_{21} = \frac{1 - 2LC\omega^2}{2Z_0\omega C} \Rightarrow \tan\phi_{21}.2Z_0\omega C = 1 - 2LC\omega^2$$

$$\Rightarrow L = \frac{1 - \tan\phi_{21}.2Z_0\omega C}{2C\omega^2}$$

B. Explanation of gate bias resistor

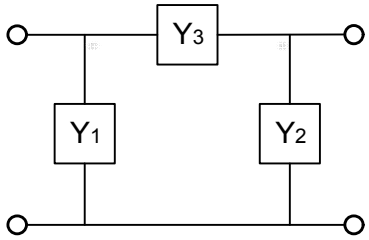


$$V_G = \frac{1}{\sqrt{1 + \frac{1}{R_G^2\omega^2C^2}}} e^{j\phi} \times V_S, \quad \phi = \tan^{-1}\left(\frac{1}{R_G C\omega}\right)$$

If R_G is not present ($R_G = 0$), $V_G \approx 0$, V_{GS} fluctuates with input swing and hence R_{ON} fluctuates. On the other hand, if the value of R_G is very large, it leads to $V_G \approx V_S$ and $V_{GS}(AC) \approx 0$, thus R_{ON} is kept unchanged. $R_G = 10\ k\Omega$ is chosen in the design.

C. Equations for choosing attenuator elements

For typical π-type 2-port network, transmission (ABCD) parameters are expressed as below:



$$A = 1 + \frac{Y_2}{Y_3}, B = \frac{1}{Y_3},$$
$$C = Y_1 + Y_2 + \frac{Y_1 Y_2}{Y_3}, D = 1 + \frac{Y_1}{Y_3}$$

From the conversion between transmission parameter (ABCD) and scattering parameter (S-parameters), S_{21}, S_{11} and S_{22} are given by:

$$S_{21} = \frac{2}{A + \frac{B}{Z_0} + CZ_0 + D}; S_{11} = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 + D}; S_{22} = \frac{-A + B/Z_0 - CZ_0 + D}{A + B/Z_0 + CZ_0 + D}$$

In case the structure is symmetrical (i.e. $Y_1 = Y_2$) and assuming impedance matching at input and output ports of the 2-port network, S_{11} and S_{22} are equal to zero or in other words,

$$\frac{B}{Z_0} = CZ_0 \Leftrightarrow \frac{1}{Y_3 Z_0} = \left(2Y_1 + \frac{Y_1^2}{Y_3}\right) Z_0 \Leftrightarrow Y_3 = \frac{1 - Y_1^2 Z_0^2}{2Y_1 Z_0^2}$$

Replacing Y_3 as a function of Y_1 and Z_0 into the expression of transmission coefficient S_{21}, it becomes: $S_{21} = \frac{1 - Y_1 Z_0}{1 + Y_1 Z_0}$. In reference state, $Y_1 = \frac{1}{R_2 + Z_{off2}}$, then

$$S_{21\_ref} = \frac{1 - \frac{Z_0}{R_2 + Z_{off2}}}{1 + \frac{Z_0}{R_2 + Z_{off2}}} = \frac{R_2 + Z_{off2} - Z_0}{R_2 + Z_{off2} + Z_0}$$

With $Z_{off2} = 1/j\omega C_{off2}$, then

$$S_{21\_ref} = \frac{1 + j\omega C_{off2}(R_2 - Z_0)}{1 + j\omega C_{off2}(R_2 + Z_0)} \Rightarrow \left|S_{21\_ref}\right| = \sqrt{\frac{1 + \omega^2 C_{off2}^2 (R_2 - Z_0)^2}{1 + \omega^2 C_{off2}^2 (R_2 + Z_0)^2}};$$
$$\phi_{21\_ref} = \tan^{-1}\left[\omega C_{off2}(R_2 - Z_0)\right] - \tan^{-1}\left[\omega C_{off2}(R_2 + Z_0)\right]$$

Inversely, in attenuation state, $Y_1 = \frac{1}{R_2 + R_{on2}}$, then

$$S_{21\_att} = \frac{1 - \frac{Z_0}{R_2 + R_{on2}}}{1 + \frac{Z_0}{R_2 + R_{on2}}} = \frac{R_2 + R_{on2} - Z_0}{R_2 + R_{on2} + Z_0}$$

Insertion loss can be defined as the below equation: $IL = 20\log\frac{1}{|S_{21}|}$. Applying to the reference state and attenuation state, they are:

$$IL_{ref} = 10\log\frac{1+\omega^2 C_{off2}^2 (R_2 + Z_0)^2}{1+\omega^2 C_{off2}^2 (R_2 - Z_0)^2}; IL_{att} = 20\log\frac{R_2 + R_{on2} + Z_0}{R_2 + R_{on2} - Z_0}$$

The difference of the insertion losses between attenuation state and reference state or attenuation level of the unit cell (in a unit of dB) is defined as:

$$A = IL_{att} - IL_{ref} = 20\log\frac{R_2 + R_{on2} + Z_0}{R_2 + R_{on2} - Z_0} - 10\log\frac{1+\omega^2 C_{off2}^2 (R_2 + Z_0)^2}{1+\omega^2 C_{off2}^2 (R_2 - Z_0)^2}$$

$$A = 10\log\left[\left(\frac{R_2 + R_{on2} + Z_0}{R_2 + R_{on2} - Z_0}\right)^2 \frac{1+\omega^2 C_{off2}^2 (R_2 - Z_0)^2}{1+\omega^2 C_{off2}^2 (R_2 + Z_0)^2}\right]$$

$$\left(\frac{R_2 + R_{on2} + Z_0}{R_2 + R_{on2} - Z_0}\right)^2 \frac{1+\omega^2 C_{off2}^2 (R_2 - Z_0)^2}{1+\omega^2 C_{off2}^2 (R_2 + Z_0)^2} = 10^{A/10}$$

The equation above demonstrates the relationship between the relative attenuation level of a unit cell and circuit parameters, expressed in terms of shunt devices. On-state resistance and off-state capacitance are known for the chosen NMOS switches, according to the attenuation level of the unit cell, denoted by A, the resistance for the shunt branch can be easily calculated.

The dependence of series branch devices on shunt branch devices is pointed out in the above equation, that is $Y_3 = \frac{1 - Y_1^2 Z_0^2}{2 Y_1 Z_0^2}$. In reference state, $Y_3 = \frac{1}{R_1} + \frac{1}{R_{on1}}$ and

$Y_1 = \frac{1}{R_2 + Z_{off2}}$, the relation becomes: $\frac{1}{R_1} = \frac{R_2 + Z_{off2}}{2Z_0^2} - \frac{1}{2(R_2 + Z_{off2})} - \frac{1}{R_{on1}}$.

Similarly, in the attenuation state, $Y_3 = \frac{1}{R_1} + \frac{1}{Z_{off1}}$ and $Y_1 = \frac{1}{R_2 + R_{on2}}$.

$\Rightarrow \frac{1}{R_1} = \frac{R_2 + R_{on2}}{2Z_0^2} - \frac{1}{2(R_2 + R_{on2})} - \frac{1}{Z_{off1}}$.