Dissertation for the Degree of Master

Studies of Power Supply Rejection Enhancement Methods for RF Power Amplifier and Low Dropout Regulator in CMOS Technology

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by

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ABSTRACT

이 논문은 주로 다중 무선 시스템의 향상된 PSR을 달성하기 위한 것입니다. 여러 무선 시스템이 포함되어 있는 콤보칩에 적합한 180-nm CMOS 의 5GHz Class-A 전력 증폭기(PA)를 설계했습니다. 설계된 2-stage 선형 전력 증폭기에는 cascode input stage와 그 출력엔 single-ended 신호를 differential 출력으로 변환시켜주는 transformer based balun이 밸런싱 캐패시터와 함께 설계되어 있습니다. Output stage에는 push-pull Class-A amplifier 와 또 다른 transformer based balun 이 differential 출력 전력을 single-ended 50Ω 부하에 효율적으로 전달합니다. 회로 내부 균형 및 differential 구성을 통해 제안된 PA 는 0.1-3.5GHz 주파수에서 9.5-65.9dB 의 power supply rejection ratio(PSRR)을 달성할 수 있습니다. 제안된 PA 의 측정 결과는 15.5dB 의 gain, 13dBm 의 output-referred 1dB gain compression point, 15.4dBm 의 output saturated power, 5MHz 의 주파수 오프셋에서 22dBm 의 output intercept point 및 15%의 peak power added efficiency 를 보여줍니다. 그리고 65-nm 의 CMOS 기술이 적용된 low dropout regulator (LDO)도 제안합니다. 제안된 LDO 는 넓은 대역폭의 높은 PSRR 을 제공하기 위해 feed-forward ripple cancellation (FFRC) 기술을 기반으로 구현되었습니다. FFRC 가 적용된 LDO 는 기본적인 LDO 에 비해 40dB 이상의 PSRR 개선을 달성했습니다.

ABSTRACT

This dissertation is mainly to achieve an enhanced PSR of the multiple wireless systems. We propose a 5 GHz class-A power amplifier (PA) in 180nm CMOS process appropriate for a radiocommunication combo-chip that can deal with multiple radio systems. The proposed two-stage linear PA contains a cascode input stage with a transformer-based balun merged with a balancing capacitor as the load in which the single-ended signal is transformed into the balanced output. Also, the PA contains an output stage push-pull class-A amplifier and another transformer-based balun which efficiently combines the differential output power to drive a single-ended 50 Ω load. The proposed PA with an internal balanced and differential configuration can attain a power supply rejection ratio (PSRR) of 9.5 to 65.9 dB at the frequency of 0.1–3.5 GHz. The proposed PA's measurement results show 15.5 dB of gain, 13 dBm of output-referred 1 dB gain compression point, 15.4 dBm of output saturated power, 22 dBm of output intercept point with a 5 MHz frequency offset, and 15% of peak power-added efficiency. We also present a low dropout regulator (LDO) with an in 65-nm CMOS technology. The proposed LDO is implemented based on the feed-forward ripple cancellation (FFRC) technique to provide a wide bandwidth of high PSRR. The designed LDO with FFRC achieved more than 40dB of PSRR improvement compared to a conventional LDO at 10 MHz.

ABBREVIATIONS

CMOS	Complementary Metal-Oxide-Semiconductor
RF	Radio Frequency
P1dB	Power 1-dB Compression Point.
DE	Drain Efficiency
PAE	Power Added Efficiency
IM	Intermodulation
P1dB	1dB Gain Compression Point
IP3	Third Order Intercept Point
LDO	Low Dropout Regulator
FFRC	Feed-Forward Ripple Cancellation
PSRR	Power Supply Rejection Ratio

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Chapter 1 INTRODUCTION

1.1 Research background

In modern integrated radio systems, enough power supply rejection (PSR) in wideband and power management is crucial. Low supply voltage noise and low interference are important for RF circuits. It is important to have very efficient power management in portable devices, on another hand stable voltage is necessary for high-speed microprocessors [1]. In order to reach these goals, a voltage regulator should be implemented on the chip. For high efficiency, switch-mode voltage regulators are taken into account because their efficiency can even be higher than 90% in practical. However, switch-mode voltage regulators need a big space for an inductor which is costly. More importantly, the intermediate DC to AC conversion in the switch-mode voltage regulator causes electromagnetic interferences (EMI). Thus, the switch-mode voltage regulator is not suited for the RF circuit which is very sensitive to the noise and interference of the supply voltage [2].

When only low dropout (LDO) regulator is used, normally power supply rejection starts to decrease at a few hundred kilohertz because of the bandwidth of the error amplifier. To have a reliable PSR at the range of megahertz and gigahertz, PSR improvements must be done in the RF power amplifier.

1.2 Research objectives

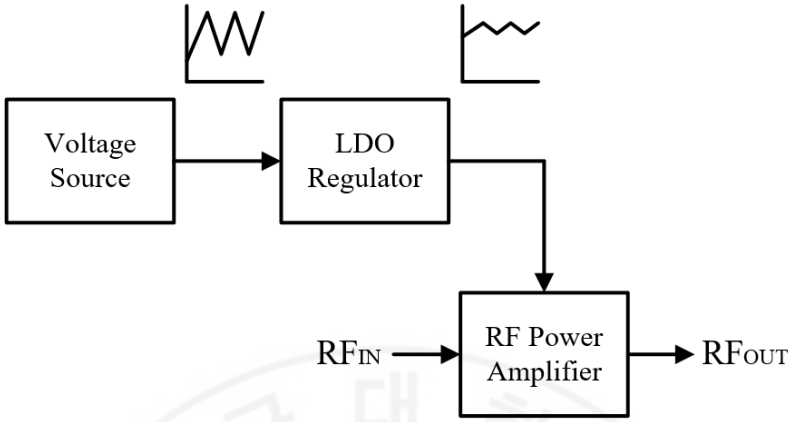

Figure 1.2-1 A block diagram of the power management system.

Figure 1.2-1 is the proposed block diagram of this dissertation. The main mechanism of the block diagram is to supply the RF power amplifier with a low dropout regulator which suppresses the noise. It is important to design a regulator with a wide range of load conditions, low quiescent current, high PSR, and low dropout voltage [3]. LDO voltage regulator is appropriate for this case.

1.3 Dissertation organization

In this dissertation, we propose a 5GHz class-A PA, a conventional LDO, and a feed-forward ripple cancellation LDO. Since the power supply noise can degrade the performance of a power amplifier [4], the proposed PA used an on-chip symmetric inductor, or a transformer balun, to improve the power supply rejection ratio, as well as to make the design compact. At the output of the first stage, the symmetric inductor with a shunt capacitor for balance converts the single-ended to a differential signal, which also works as an inter-stage matching network. Then, the second balun combines the output power of the differential common source amplifier to converts

the output port from the differential to a single-ended system. With this circuit structure, the proposed PA can attain significantly improved radio frequency power supply rejection under multiple wireless-system scenarios while delivering reasonable performance. The PA has 15.4 dBm of saturated power output and 15% of peak PAE. The implemented PA utilizes only 0.65 mm^2 of circuit area without pads, because of the transformer-based compact baluns.

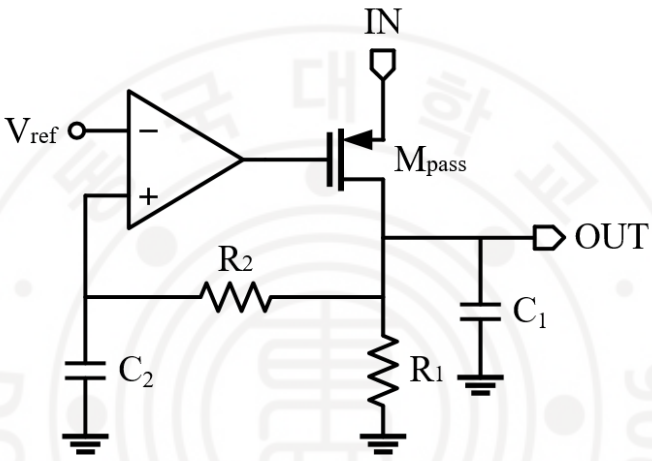

Figure 1.3-1 A schematic diagram of the conventional LDO.

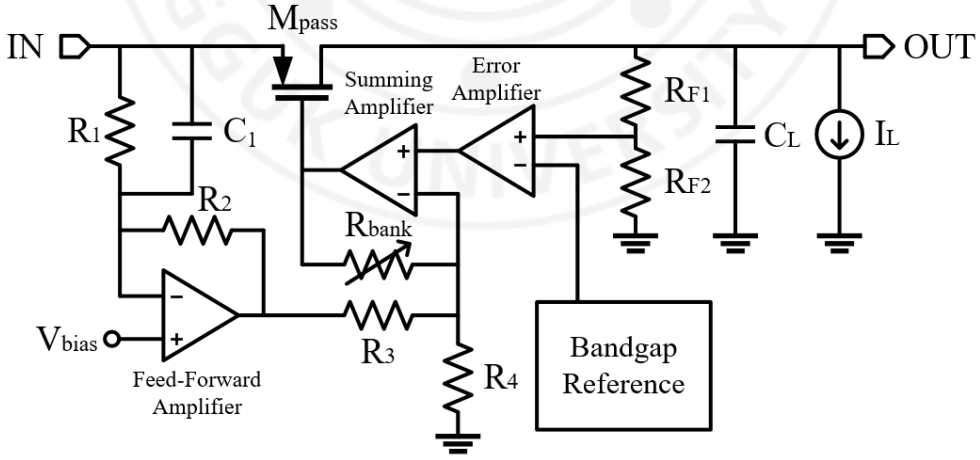

Figure 1.3-2 A schematic diagram of the FFRC LDO.

The voltage regulator that is suitable to provide a clean voltage source is a low dropout voltage regulator due to the wide range of load conditions, low quiescent current, high PSR, and low dropout voltage. In chapter 3, two LDOs are proposed with 65nm CMOS technology. One LDO is a conventional PMOS LDO which is shown in Figure 1.3-1. Another is a feed-forward ripple cancellation (FFRC) LDO which is shown in Figure 1.3-2.

Chapter 2 POWER AMPLIFIER

2.1 Power Amplifier

In radiocommunication for mobile applications, a power amplifier (PA) is a key block in the radio frequency (RF) front-end. The PA must not only carry the necessary power efficiently but also should be strong enough towards the common-mode interferences from surrounding blocks. Especially, a robust design to manage the interference should be attained in multiple radio applications, since diverse wireless systems are implemented in a single chip. A PA requires many design trade-offs between the supply voltage, linearity, output power, and power efficiency, to meet the desired specifications. Many researchers have put huge efforts and showed significant interest in enhancing the linearity, improving the efficiency of PAs, lowering power consumption, and decreasing the cost [5,6]. Even though a switching power amplifier theoretically has 100% of the drain efficiency, it is not possible to be used on the modulation scheme, which utilizes the transmitting signal's amplitude. To solve this issue, a polar power amplifier has been designed using a mixed-signal technique [7]. However, the size of the reference mixed-signal 2.4 GHz PA is too bulky (3.06 mm^2), because of the extra radio frequency digital-to-analog converter, DAC, for the polar operation. Moreover, the switching PA may create large interferences from the digital blocks, which can seriously spoil the sensitive analog/RF blocks which are integrated onto the same chipset.

The linearity of the PA directly affects the whole system. Orthogonal frequency-division multiplexing (OFDM) is frequently used to supply fast data rates at 5 GHz in IEEE 802.11a wireless LAN applications. Since the linearity of the power amplifier controls the data rates of the communication, a high linear power amplifier

is necessary [8]. In contrast, a linear PA can support any modulation schemes. Among linear power amplifiers, the class-A power amplifier has the greatest linearity and smallest distortion, which are essential features for radio communication [5,6]. By using a differential structure, the class-A PA can also attain an outstanding common-mode rejection. And with an inductive load, the power amplifier will have a relatively good power-added efficiency (PAE). For that reason, class-A PAs have been frequently used in this field, especially in WLAN transceivers [9]. But, a normal single-ended power amplifier has a bad common-mode rejection, which is not a good idea to implement into a combo-chip with multiple wireless circuits integrated on the same chipset.

Power amplifiers are classified into two categories: Linear PA (Class-A, Class-B, Class-AB, Class-C) and switch-mode PA (Class-D, Class-E, and Class-F PA). Only linear power amplifiers will be presented.

2.1.1 Linear Power Amplifiers

Figure 2.1-1 shows a generic topology for linear power amplifiers. Class-A, Class-B, Class-AB, and Class-C are called the linear power amplifiers because the output of the linear power amplifier is related and proportional to the input. Class-A power amplifier is the only one that is fully linear among the group of classes while sacrificing power efficiency. The rest of the power amplifiers give up linearity to enhance efficiency. They reduced the conduction angle to let the active devices turn on at certain parts of the cycle. Table 2.1-1 explains the difference in conduction angle and maximum drain efficiency (DE) of the linear power amplifiers. Figure 2.1-2 shows the efficiency of a power amplifier as a function of the conduction angle.

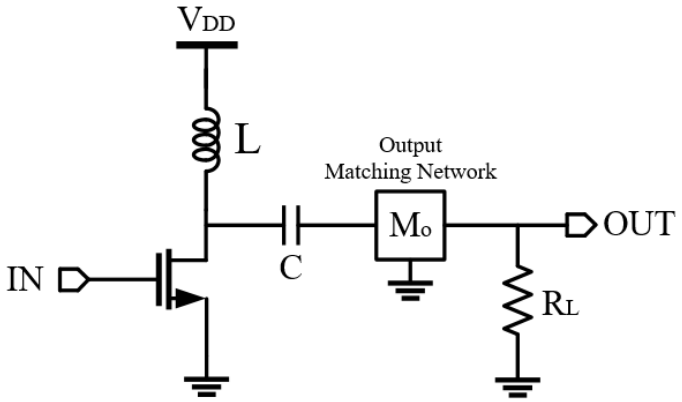

Figure 2.1-1 A schematic diagram of a linear power amplifier.

Table 2.1-1 Comparison of the linear power amplifiers.

Class	Conduction Angle	Maximum DE
A	θ=360°	50%
AB	180°<θ<360°	50~79%
B	θ=180°	79%
C	0°<θ<180°	79~100%

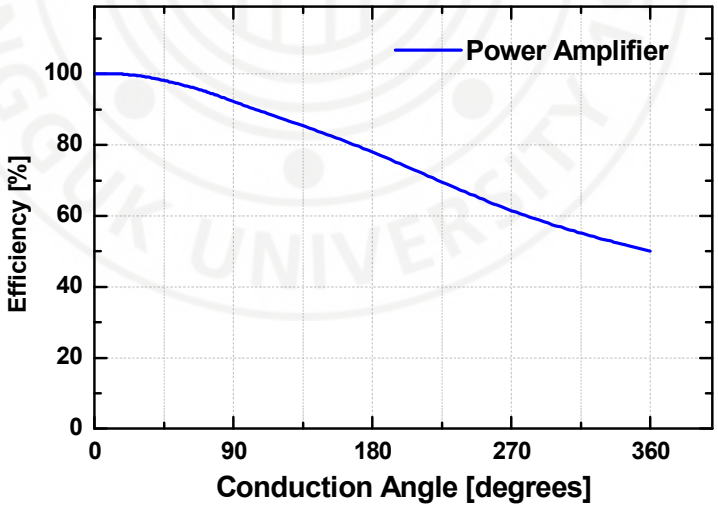

Figure 2.1-2 Efficiency of a power amplifier as a function of the conduction angle.

2.1.1.1 Class-A Power Amplifier

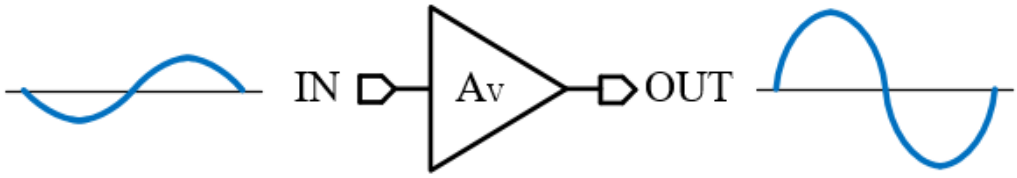

Figure 2.1-3 Input and output voltage swing of a Class-A power amplifier.

Class-A power amplifiers have a high gain and linearity. The conduction angle for a class-A power amplifier is 360 degrees which is shown in Figure 2.1-2. So, the class-A power amplifier has the highest linearity than other classes. The 360 degrees conduction angle means that the class-A power amplifier is always ON, which leads to low power efficiency. Theoretically, class-A power amplifiers can reach up to 50% of drain efficiency [10].

2.1.1.2 Class-B Power Amplifier

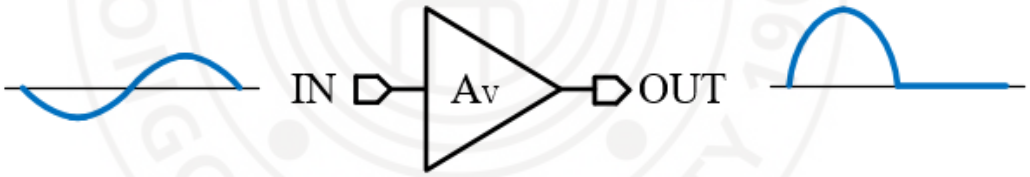

Figure 2.1-4 Input and output voltage swing of a Class-B power amplifier.

For class-B power amplifiers, the conduction angle is 180 degrees which is half of class-A's conduction angle which is shown in Figure 2.1-3. This is because class-B power amplifiers are turned ON only half of the period. Therefore, two MOSFETs are used for class-B power amplifiers to each cover the half of the period. The linearity decreased compared to a class-A power amplifier, but the efficiency is increased to about 79% [10].

2.1.1.3 Class-AB Power Amplifier

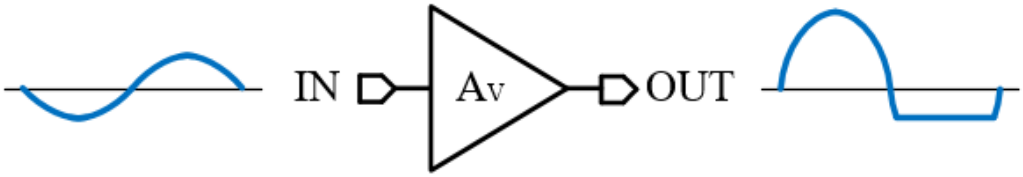

Figure 2.1-5 Input and output voltage swing of a Class-AB power amplifier.

Class-AB power amplifiers are named "AB" because it stays somewhere between class-A and class-B power amplifiers. The conduction angle of class-AB power amplifiers is between 180 to 360 degrees which is shown in Figure 2.1-4. The linearity also remains in between; which means that class-AB power amplifiers are more linear than class-B but less linear than class-A. Efficiency is also in the same story [10].

2.1.1.4 Class-C Power Amplifier

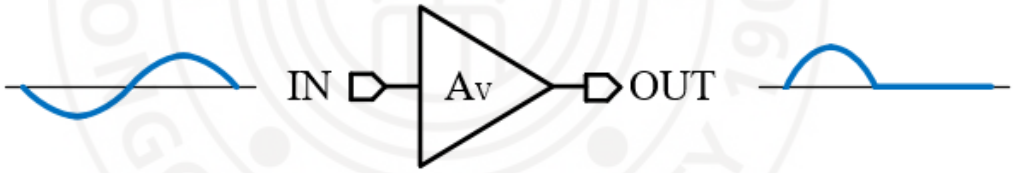

Figure 2.1-6 Input and output voltage swing of a Class-C power amplifier.

Class-C power amplifiers' conduction angle is less than 180 degrees which is shown in Figure 2.1-5, so it becomes more nonlinear and more efficient. If the conduction angle reaches zero degrees, the efficiency of the power amplifier reaches 100%. Therefore, class-C power amplifiers provide high efficiency only if it is turned ON for a very short period [10].

2.2 Efficiency

Because power amplifiers are one of the most current consuming blocks, power efficiency is important. Power efficiency is how well power is delivered through the power amplifier [11]. When talking about power efficiency in power amplifiers, drain efficiency and power added efficiency is always considered.

Drain Efficiency (DE) is the ratio between the radio frequency (RF) output power over dissipated power. Input power is not covered in DE. The equation for drain efficiency is

$$DE = \frac{P_{RFout}}{P_{diss}} \times 100\% \qquad (2.2\text{-}1)$$

Where P_{RFout} is the RF output power and P_{diss} is the dissipated power.

Power Added Efficiency (PAE) is the most used measure when people talk about efficiency in power amplifiers. PAE is similar with DE but with the input power. The equation for power added efficiency is

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{diss}} \times 100\% \qquad (2.2\text{-}2)$$

Where P_{RFin} is the RF input power.

2.3 Linearity

Linearity is an important factor in modern wireless communications [12]. By improving the linearity, the interference created will be minor. If the circuit is non-linear, undesired distortions in signal will happen and ruin the whole chain system. The more linear the power amplifier is, the better protected output. This means that assuring linearity in a circuit is first then efficiency follows.

A nonlinear power amplifier becomes a problem if the signals are modulated. Intermodulation (IM) is discussed when linearity is explained. Intermodulation

distortion (IMD) is the amplitude of the distorted signal produced by two or more different frequency signals. Third order intermodulation distortion (IMD3) is commonly considered in intermodulation. IMD3 is the difference between the fundamental signal and the IM3.

Shown in Figure 2.3-1, third order intercept point (IP3) is the point where the fundamental signal and the IM3 signal become equal considering that both signals do not saturate and increase continuously. IP3 is the first to talk about linearity. The IM3 signal increases three times the fundamental signal in log scale. This is the reason that IM3 is a threat to linearity. Practically, both signals never meet each other because they get saturated at a certain point.

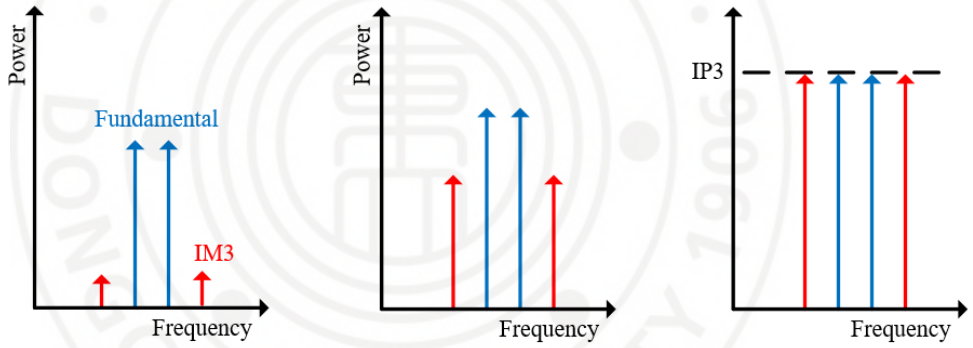

Figure 2.3-1 A schematic diagram of a linear power amplifier.

2.4 Passive elements

In RF circuits, there are many passive elements that must be used on chip. The active devices of the power amplifier are controlled by passive elements. In this dissertation, transmission lines-CPW, inductors, and transformers will be considered. They are directly implemented on chip to avoid additional parasitic capacitance and loss when it is not on the chip.

2.4.1 Coplanar Waveguide (CPW)

Coplanar waveguides, one type of transmission line, are used in connecting stages and other blocks in a RF circuit [10]. The signal path is surrounded by ground planes so that it can carry the signal with the least amount of loss. The CPW is designed in the HFSS tool and set up to transfer a balanced signal.

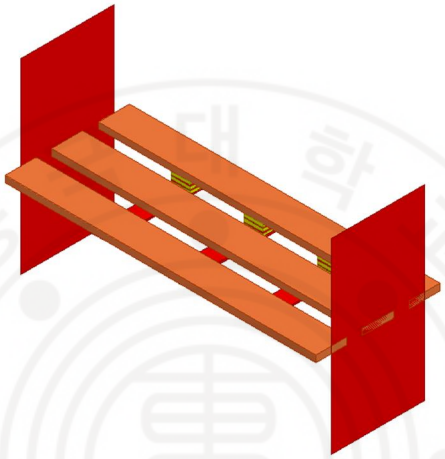

Figure 2.4-1 A HFSS diagram of the coplanar waveguide.

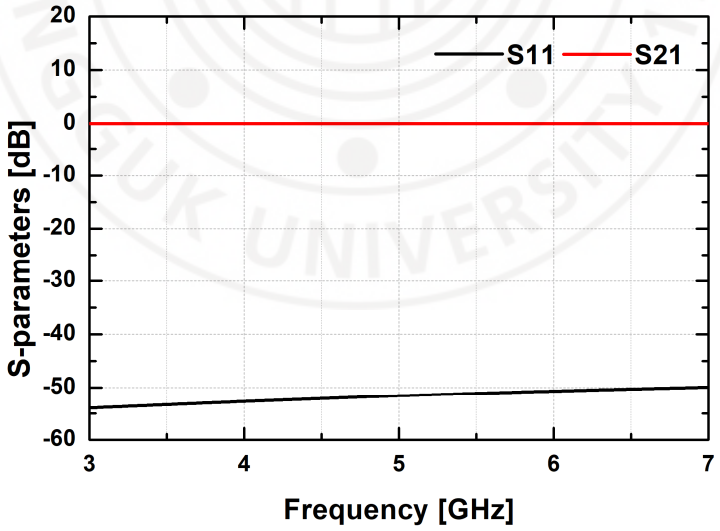

Figure 2.4-2 S-parameter simulation of the coplanar waveguide.

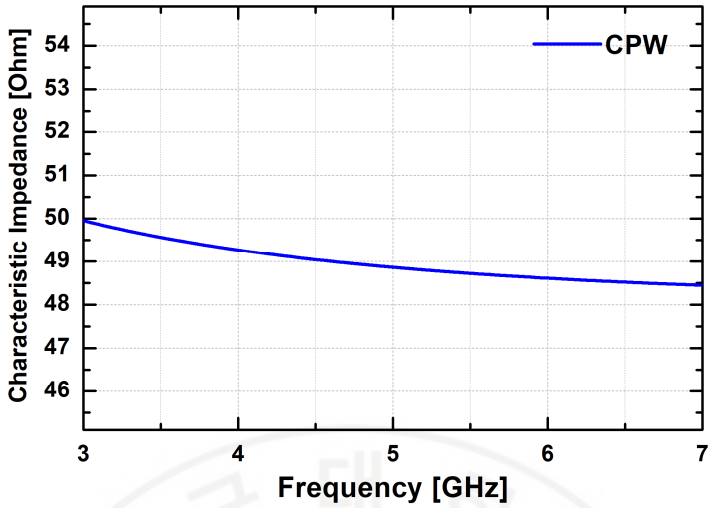

Figure 2.4-3 Characteristic impedance of the coplanar waveguide.

Figure 2.4-1 is a diagram of a coplanar waveguide in HFSS. With the CPW design, the simulated S-parameter and characteristic impedance are shown in Figure 2.4-2 and 2.4-3. The signal passes through the CPW with almost no loss. The characteristic impedance ensures that if the CPW is connected to a 50 Ohm load, there will be almost no reflection.

2.4.2 Inductor

Inductors are implemented onto chips as a spiral form. Normally inductors are realized in the top metal layer because it is the thickest metal. Making an inductor with the top metal layer helps minimize the resistance across the inductor and the parasitic capacitance. Quality factor, Q, must be considered when designing an inductor in a RF circuit. The equation for quality factor can be express by

$$Q = \frac{L \times \omega_0}{R} \qquad (2.4.2\text{-}1)$$

where $L \times \omega_0$ stands for the inductance and R stands for the resistance of the inductor [10].

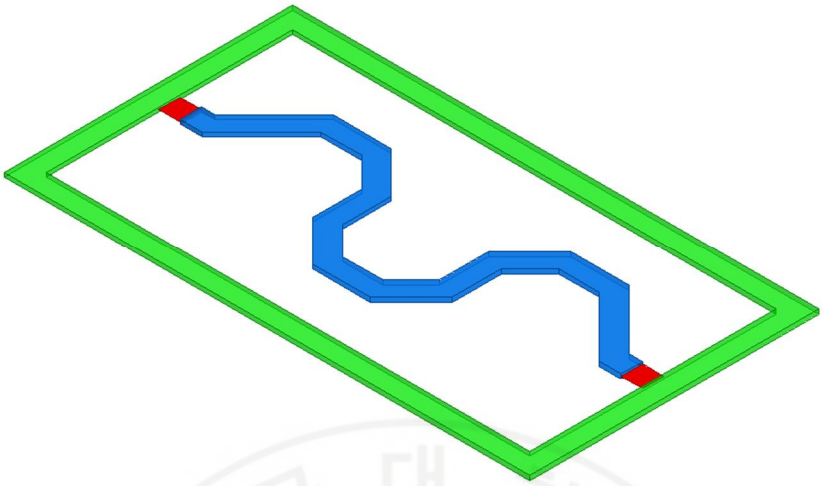

Figure 2.4-4 A HFSS diagram of the source degeneration inductor.

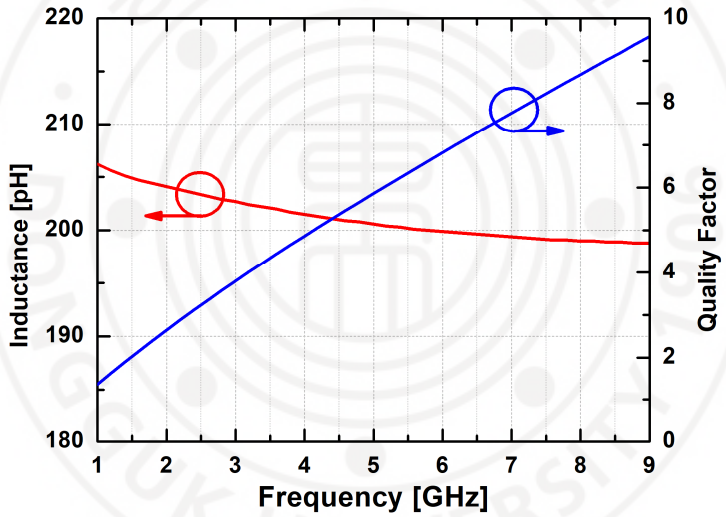

Figure 2.4-5 Simulation results of the inductance and quality factor of the source degeneration inductor.

Figure 2.4-4 shows the source degeneration inductor that is used in the proposed 5GHz power amplifier. Figure 2.4-5 is the simulation results of the inductance value and quality factor with HFSS. The inductor has about 200 pH of inductance and 6 of quality factor.

Figure 2.4-6 shows the symmetric inductor (balun) that is used in the proposed 5GHz power amplifier. Figure 2.4-7 is the simulation results of the inductance value

and quality factor with HFSS. The blue part of the symmetric inductor is the primary loop and the red part is the secondary loop. The inductance of primary and secondary loop is both 1.425 nH at 5 GHz. The quality factor of the primary and secondary loop is 10.2 and 9.4. The difference in Q happened because the second loop has two bridges in the path using a thinner metal layer, M5, than the thick metal, TKM (M6). This led to making the secondary loop more resistive and made the quality factor lower [13]. Reference [10] mentions about symmetric inductors and the benefits of using it. Because it is a combination of two spiral inductors, symmetric inductors save area and also has a higher quality factor.

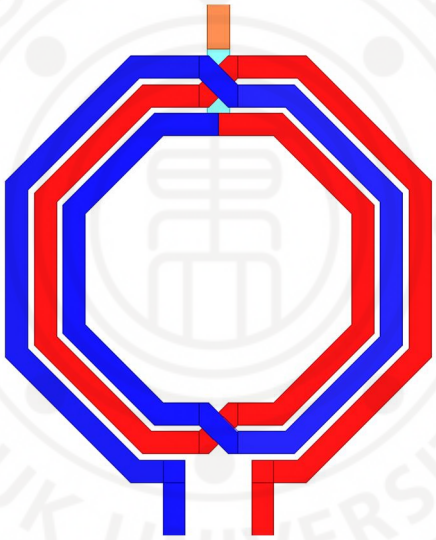

Figure 2.4-6 A HFSS diagram of the symmetric inductor (balun).

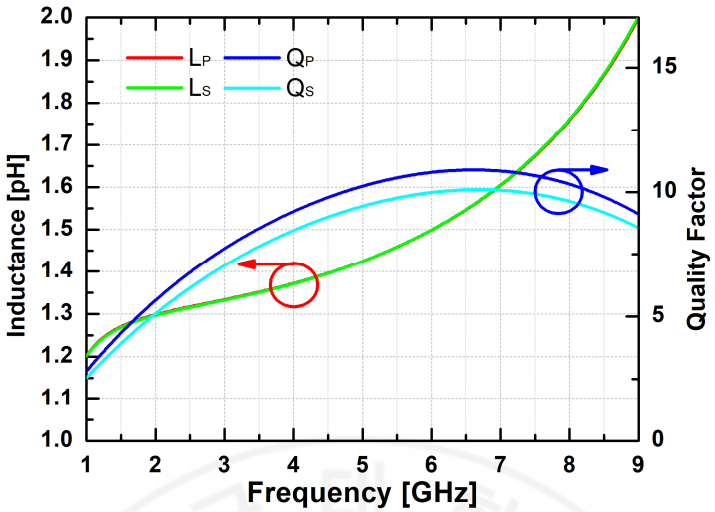

Figure 2.4-7 Simulation results of the inductance and quality factor of the symmetric inductor (balun).

2.4.3 Transformer

Transformers are very important in RF circuits because of its usages: perform impedance matching, change a single-ended signal to differential output or vice versa, and perform ac coupling between stages [10]. Same with inductors, it is best to use the top metal layer because of its thickness and low parasitic capacitance between the metal and the substrate. Other than that, transformers must have high magnetic coupling between the primary and secondary spiral and low capacitive couple between them.

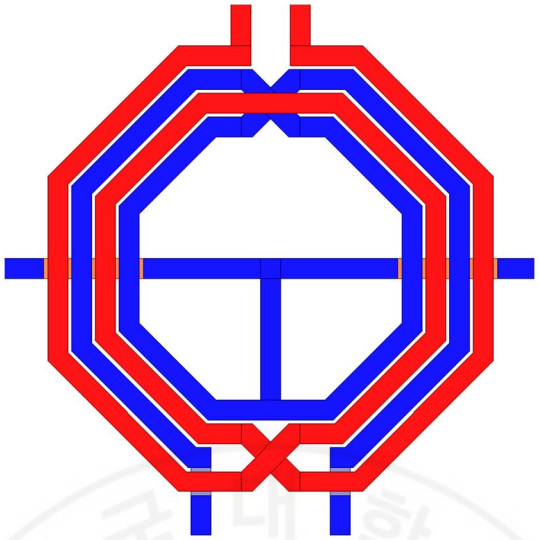

Figure 2.4-8 A HFSS diagram of the transformer.

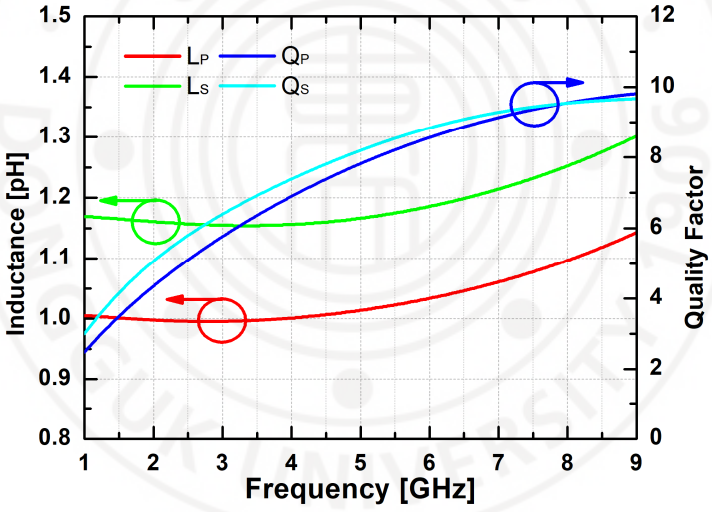

Figure 2.4-9 Simulation results of the inductance and quality factor of the transformer.

Figure 2.4-8 shows the transformer that is used in the proposed 5GHz power amplifier. Figure 2.4-9 is the simulation results of the inductance value and quality factor with HFSS.

2.5 Proposed Power Amplifier

Providing enough power supply rejection (PSR) in a broadband range is one of the critical design considerations in modern integrated multiple radio systems. To achieve an enhanced PSR of the multiple wireless systems, the proposed 5 GHz class-A power amplifier (PA) in 180nm CMOS process is applicable for a radiocommunication combo-chip that can deal with multiple radio systems. The proposed two-stage linear PA contains a cascode input stage with a transformer-based balun merged with a balancing capacitor as the load in which the single-ended signal is transformed into the balanced output. Also, the PA contains an output stage push-pull class-A amplifier and another transformer-based balun which efficiently combines the differential output power to drive a single-ended 50 Ω load.

The circuit schematic of the proposed power amplifier as shown in Figure 2.5-1.

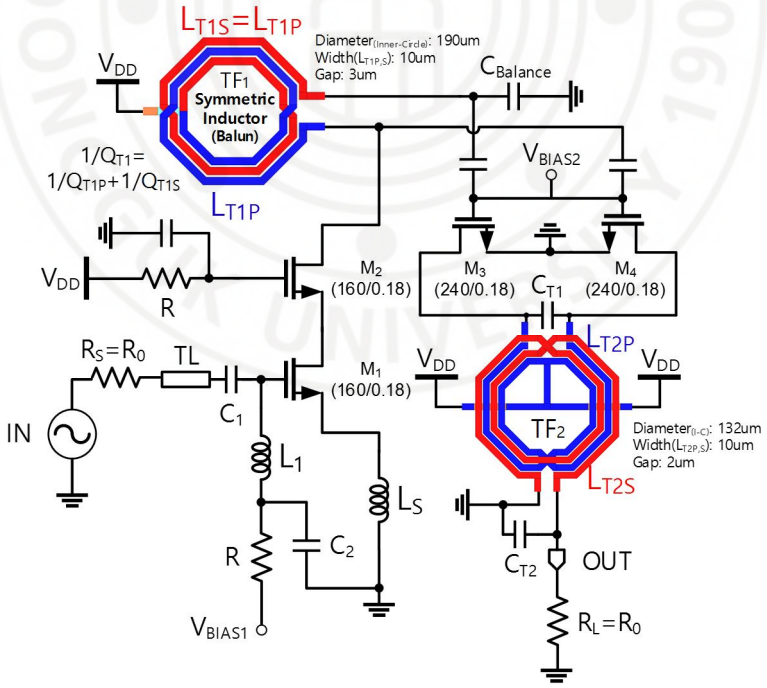

Figure 2.5-1 A schematic diagram of the proposed power amplifier.

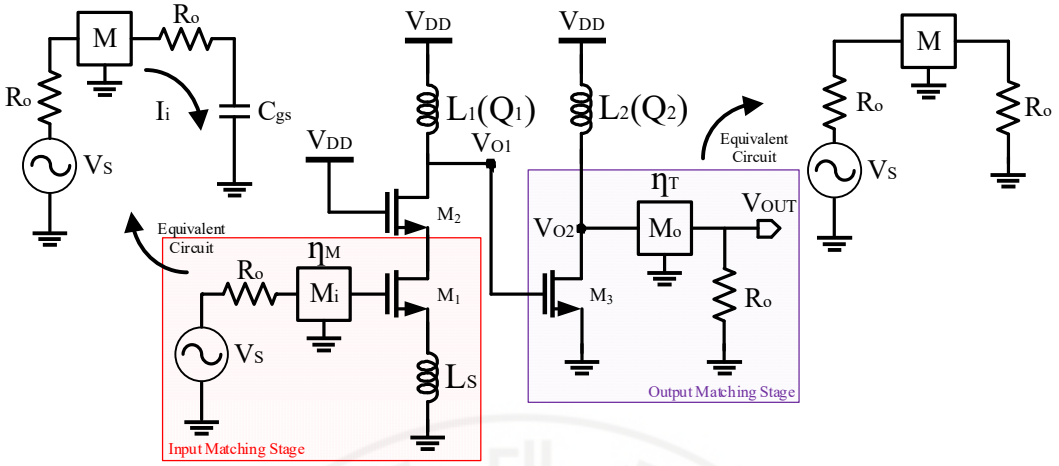

Figure 2.5-2 A simplified diagram of the proposed power amplifier.

The Figure 2.5-2 represents the simplified schematic version of the proposed power amplifier. In the input matching stage (red region), the available input power, P_i, can be calculated as

$$P_i = (\frac{V_s}{2})^2 \cdot \frac{1}{R_o} = \frac{V_s^2}{4R_o} \tag{2.5-1}$$

The input matching stage (red region) can be expressed as the equivalent circuit. The V_i and V_{gs} can be determined by the following equations 2.5-2 and 2.5-3.

$$V_i = \frac{V_s}{2R_o} \text{ at } \omega_0 \tag{2.5-2}$$

$$V_{gs} = \frac{V_s}{2R_o} \cdot \frac{1}{sC_{gs}} = \frac{V_s}{2} Q_i \tag{2.5-3}$$

The effective G_m can be expressed as equation 2.5-4.

$$G_m = \frac{g_{m1}}{1 + g_{m1}(sL_s)} \tag{2.5-4}$$

Then, the voltage gain V_{o1}/V_i can be calculated by

$$\left|\frac{V_{o1}}{V_i}\right| = \left|G_m R_L\right| \text{, where } R_L = \omega_0 L_1 Q_1 \tag{2.5-5}$$

V_{o1} and V_{o2} in Figure 2.5-2 can be calculated as

$$V_{o1} = \frac{Vs}{2} \cdot \frac{g_{m1} Q_i}{1 + g_{m1}(sL_s)} \cdot \omega_0 Q_1 L_1 \tag{2.5-6}$$

$$V_{o2} = g_{m2} \cdot (\omega Q_2 L_2 \| r_{o2}) \cdot V_{o1} \tag{2.5-7}$$

$$P_o = \eta_M \eta_T \cdot \frac{1}{R_{o2}} \cdot \left(\frac{V_{o2}}{2}\right)^2 \tag{2.5-8}$$

The proposed PA is a two-stage amplifier with the cascode stage with the source degeneration inductor as the 1st stage, and the common-source amplifier as the 2nd stage in differential mode. At the center frequency f_o ($f_o=\omega_o/2\pi$), the derived transducer power gain (G_T) is given by equation 2.5-9.

$$G_T = \frac{P_L}{P_{avs}} \approx \eta_M Q_i^{\,2} R_o \left[\frac{\left(g_{m1} Q_{T1} \omega_o L_{T1P}\right)^2}{1 + \left(g_{m1} \omega_o L_S\right)^2}\right]\left[\frac{g_{m2}^{\,2} r_{o3} Q_{T2P} \omega_o L_{T2P}}{r_{o3} + Q_{T2P} \omega_o L_{T2P}}\right]\eta_T \tag{2.5-9}$$

$$\eta_M = \frac{1}{1 + \frac{r}{Q_i^2}} \tag{2.5-10}$$

$$\eta_T = \frac{1}{1 + \frac{2}{Q_{T2P} Q_{T2S} k^2} + 2\sqrt{\frac{1}{Q_{T2P} Q_{T2S} k^2}\left(1 + \frac{1}{Q_{T2P} Q_{T2S} k^2}\right)}} \tag{2.5-11}$$

where R_o is the source and load impedance, $Q_i = 1/\omega C_{gs1} R_o$, Q_{T1} is the quality factor (Q-factor) of the 1st transformer (TF_1), η_M, and η_T are the power efficiency of the input (L-matching) and output (TF_2) matching networks, respectively [24], the resistance transformation ratio $r=R_o/R_e\{Z_{in}\}=1$, k is the magnetic coupling coefficient, Q_{T2P} and Q_{T2S} is the Q-factor of the primary and secondary coil of the TF_2.

The circuit layout of the proposed power amplifier as shown in Figure 2.5-3.

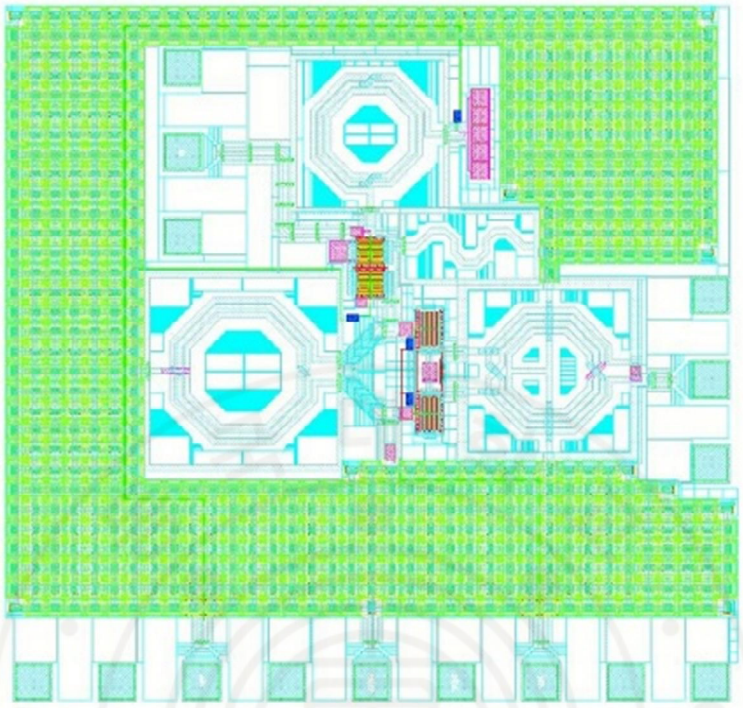

Figure 2.5-3 The full chip layout of the PA.

Figure 2.5-3 shows the microphotograph of the propose 5 GHz power amplifier in 65nm CMOS process.

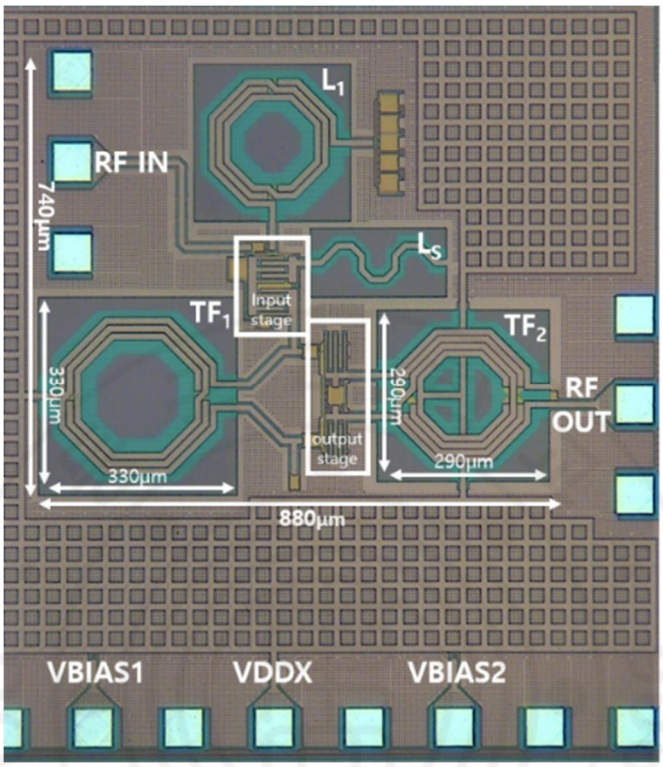

Figure 2.5-4 The microphotograph of the proposed PA.

The system layout includes:

(1) Cascode Stage (Input Stage)

(2) Common Source Stage (Output Stage)

(3) Biasing Inductor L_1

(4) Source Degeneration Inductor L_S

(5) Symmetric Inductor TF_1 (Balun)

(6) Differential to Single-Ended Transformer TF_2

Chapter 3 LOW DROPOUT REGULATOR

3.1 Introduction to Regulators

IC designers agree that voltage regulation is a key point in integrated circuits. The main purpose of a voltage regulator is to lower the noise and interference in the supply voltage for other blocks in a chip. Especially in a mixed IC, interferences created by digital circuits can be critical for analog circuits. In designing a voltage regulator circuit, several factors must be considered.

First, dropout voltage should be considered because it determines the required voltage for the unregulated power supply. If the dropout voltage is low, the unregulated power supply voltage can be lower which will lower the power dissipation of the regulator.

Second, area of the voltage regulator should be small as possible. In a single chip, there will be many circuits that need voltage regulation for their power supply. If the size of the voltage regulator is small, it will be easier to assemble with other circuits. Less space means more devices can fit on a wafer which will lead to decreasing the cost of manufacture.

Third, bandwidth of power supply rejection ratio must be considered. If the bandwidth is large enough, it means that the regulator can maintain its power supply rejection until the frequency of the bandwidth.

Lastly, stability must be considered. As mentioned earlier, the main purpose of a voltage regulator is to lower the noise and interference in the supply voltage so the voltage regulator must provide a stable voltage to other blocks. Because stability changes with different load conditions, a regulator should be designed so that it has a good phase margin for a variety of loads [14].

For researchers in the power management system, the demand for integrating the whole power management integrated circuit (PMIC) into a single chip have increased [3]. By integrating the power management system into a chip, the cost has been saved for not using the power management blocks outside of the chip. However, when the PMIC is integrated on chip, the frequency bandwidth must be increased. For the voltage regulators, the bandwidth of the circuit should be wider than before and must provide higher power supply rejection (PSR) according to the surrounding blocks. Conventional low dropout regulators (LDO) provide poor PSR at higher frequencies like 300 KHz [3].

Various techniques have been introduced to improve the PSR. By using a RC filter at the output of the LDO or using two regulators will help improve the PSR [25]. This technique can improve the PSR, but it also increases the dropout voltage because of the series resistor or the second regulator. Another technique is using a charge pump and a NMOS pass transistor [26]. This method utilizes a NMOS pass transistor which requires that the bias of the NMOS should be higher than the supply voltage. Reference [26] implemented a charge pump in order to provide the higher bias which is an independent bias for the regulator. However, this technique dissipates more dc power and increases the complexity of the circuit.

In this paper, we introduce a LDO regulator which achieves a significantly improved PSR by utilizing the feed-forward ripple cancellation technique. The purpose of this technique is to duplicate the input ripples to the gate of the pass transistor so that it will cancel out the input ripples to increase the power supply rejection significantly. The proposed LDO consists of a three-stage error amplifier (EA), a summing amplifier (SA), and a feed-forward amplifier (FFA), which helps

to increase the PSR and provide a robust output voltage. To precisely control the gain of the summing amplifier, we employ a variable resistor consisting of MOS switches and binary resistive bank which can change the total resistance linearly with the control bits. The feed-forward ripple cancellation technique will be covered in detail on chapter 3.5.

This chapter will cover the basic theories of voltage regulators, the power supply rejection ratio, the load and line regulation, the conventional low dropout regulator, and the proposed feed-forward ripple cancellation low dropout regulator. Voltage regulators can be categorized into two groups: switching regulator and linear regulator.

3.1.1 Switching Regulators

Switching regulators are normally much more efficient than linear regulators because of its method of operation. When the switch is ON, high current flows across with no voltage difference between input and output. When the switch is OFF, it will have high voltage difference between input and output but with zero current flowing. This mechanism will lead to almost zero power consumption. Switching regulators also have the benefit to have a larger output voltage than the input voltage.

However, there are two critical disadvantages when using a switching regulator. One disadvantage is that the switching can cause another interference to other circuits. Another disadvantage is that it requires more area than linear regulators. Figure 3.1.1-1 shows what a switching regulator needs: a controller with an oscillator, pass element, an inductor, capacitors, and diodes. When inductors are integrated in the circuit, the total size of the regulator will be huge [15].

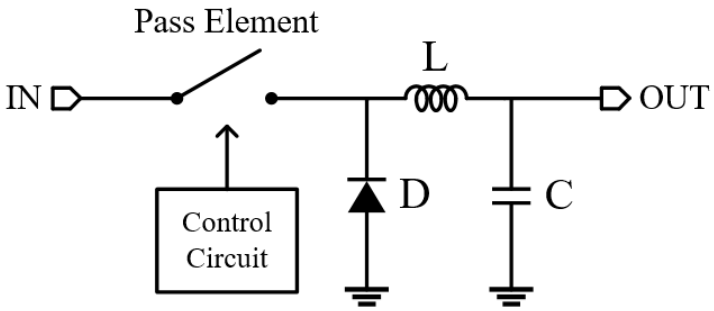

Figure 3.1-1 Switching regulator.

3.1.2 Linear regulators

To overcome the disadvantages of the switching regulators, a linear voltage regulator must be used for analog or RF circuits. Although linear regulators are not efficient as switching regulators, linear regulators are smaller in size, have less voltage ripple at the output, and are more stable with different loads.

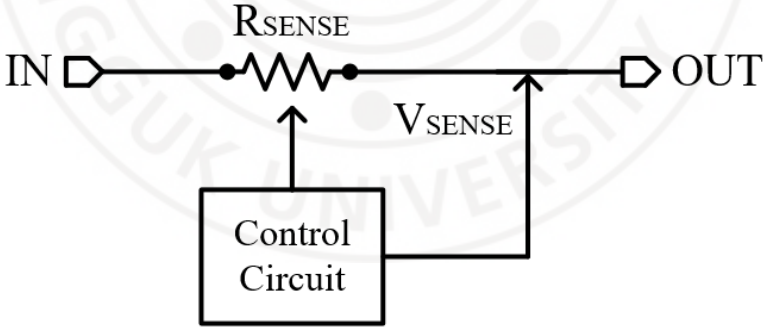

Figure 3.1-2 Linear regulator.

Figure 3.1-2 represents standard design of a linear regulator. MOSFET is used as a sense resistor to have a defined output voltage. Then the control circuit senses

the output voltage and controls the current flowing through the sense resistor to make sure that the output voltage stays stable [15].

3.1.2.1 Low Dropout Linear Regulators

The low dropout regulator (LDO) is the most efficient type of linear regulator. Dropout voltage means the voltage drop between input and output voltage. Power efficiency becomes higher if the dropout voltage is lower.

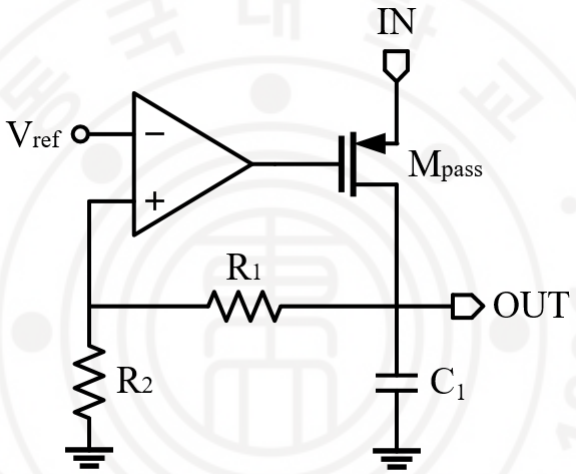

Figure 3.1-3 The schematic diagram of the conventional LDO.

3.2 Power Supply Rejection Ratio, PSRR

Power supply rejection ratio, PSRR, is how much the circuit can reject the noise and interference from the voltage source.

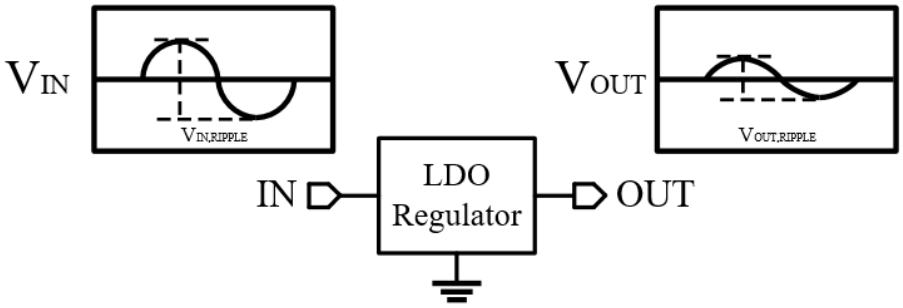

Figure 3.2-1 The block diagram of LDO.

$$PSRR[dB] = 20\log\frac{\Delta Vin, ripple}{\Delta Vout, ripple}[dB] \quad (3.2\text{-}1)$$

Figure 3.2-1 simply shows that the ripple in the input voltage will decrease after the LDO regulator circuit. Equation 3.2-1 is how to calculate the PSRR in dB. Vin,ripple represents the noise and interference and Vout,ripple is the regulated output voltage [16].

3.3 Load/Line Regulation

Load regulation is the capability to keep a constant voltage level despite the changes in the supply's load. The equation of load regulation is given by,

$$Load\ Regulation = \frac{\Delta Vout}{\Delta IL}[mV/mA] \quad (3.3\text{-}1)$$

Line regulation is the capability to keep a constant voltage despite the changes in the input voltage. Dropout voltage will vary proportionally to the change in input voltage. The equation of line regulation is given by,

$$Line\ Regulation = \frac{\Delta Vout}{\Delta Vin}[V/V] \quad (3.3\text{-}2)$$

3.4 Conventional Low Dropout Regulator (LDO)

Figure 3.4-1 is the basic schematic diagram of a low dropout regulator. The basic operation of an LDO regulator is based on the feed-back. The feed-back will control the current flow of the power transistor. Figure 3.4-2 is the used two-stage operational transconductance amplifier (OTA) schematic in transistor-level. The first stage is a differential amplifier with an active load and the next stage is a common source amplifier. The transistor size is in micro-meters. Bias voltages V_{CAS} and V_S are applied directly from external voltage supplies through the on-chip pad which is shown in Figure 3.4-2.

The output voltage will be fixed to a regulated voltage level by V_{ref}, R_1, and R_2 [17].

$$V_{output}[V] = V_{ref} \times \frac{R_1 + R_2}{R_2}[V] \tag{3.4-1}$$

Equation 3.4-1 shows how V_{output} is fixed with V_{ref}, R_1, and R_2.

The operational transconductance amplifier (OTA) has some characteristics. First, it is a single-pole amplifier with a high gain. The OTA also has a trade-off between gain and bandwidth. Lastly, the main part of the OTA is that it is stable for all gain values. Stability means that there is a ringing effect at the closed-loop output of the amplifier. So, the phase margin of the OTA should be 45 degrees or more to have a stable output.

In this design, the two-stage OTA has three left half plane poles (LHP) and a right half plane zero (RHZ). The first dominant pole is the miller pole which can be expressed as equation 3.4-2.

$$P_1 = \frac{-(g_{ds2} + g_{ds4})(g_{ds5} + g_{ds8} + g_{ds9})}{g_{m5} C_c} \tag{3.4-2}$$

The next non-dominant LHP is the output pole expressed as equation 3.4-3.

$$P_2 = \frac{g_{m5}}{C_L} \tag{3.4-3}$$

where C_L is the load capacitance of the OTA. The third LHP is the mirror pole at the first stage of the OTA.

$$P_3 = \frac{-g_{m3}}{C_M} \tag{3.4-4}$$

where C_M is the total capacitance between M1, M3, and M4.

The RHZ can be expressed as equation 3.4-5.

$$Z_1 = \frac{g_{m5}}{C_C} \tag{3.4-5}$$

This RHZ is not desired for an OTA because the magnitude increases while the phase decreases in a bode plot. To reduce the RHZ's effect, a series resistor R_{gd} is added to make a left half plane zero (LHZ) to compensate the RHZ.

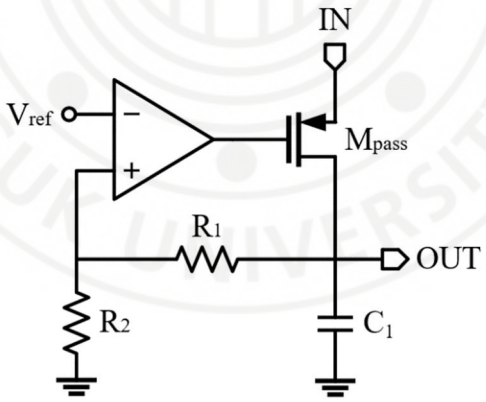

Figure 3.4-1 The schematic diagram of the conventional LDO.

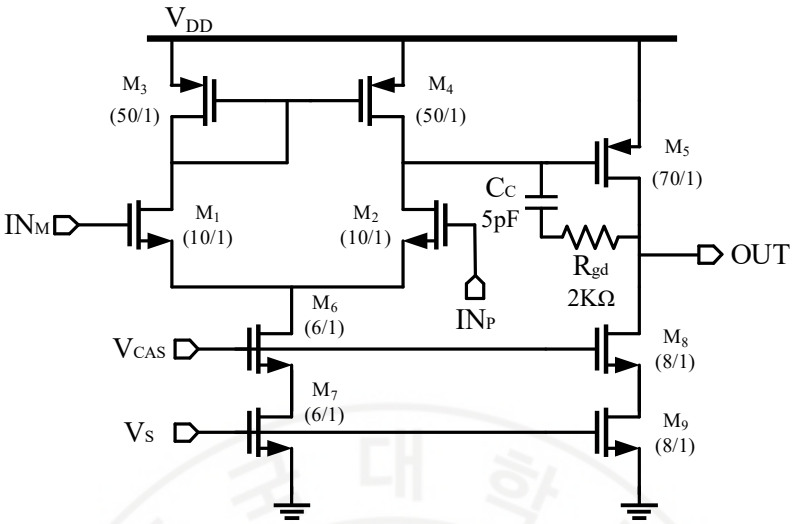

Figure 3.4-2 Transistor-level schematic of the OTA.

The conventional LDO has been designed in 65-nm CMOS process. Figure 3.4-3 shows the chip layout of the conventional LDO. It is designed so that the input voltage (VDD) is 1.2V and the output regulated voltage as 1V and 1.05V.

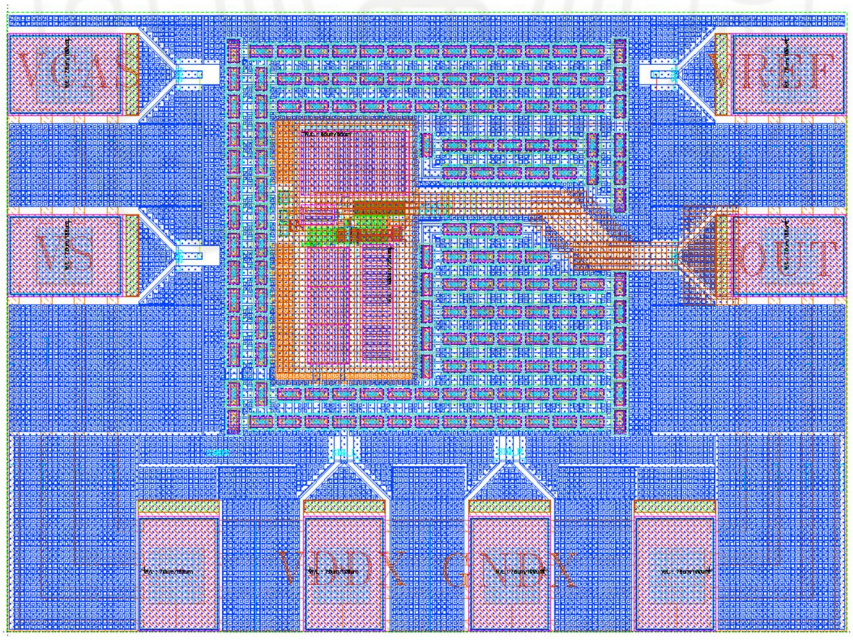

Figure 3.4-3 The full chip layout of the conventional LDO.

3.5 Feed-Forward Ripple Cancellation LDO (FFRC)

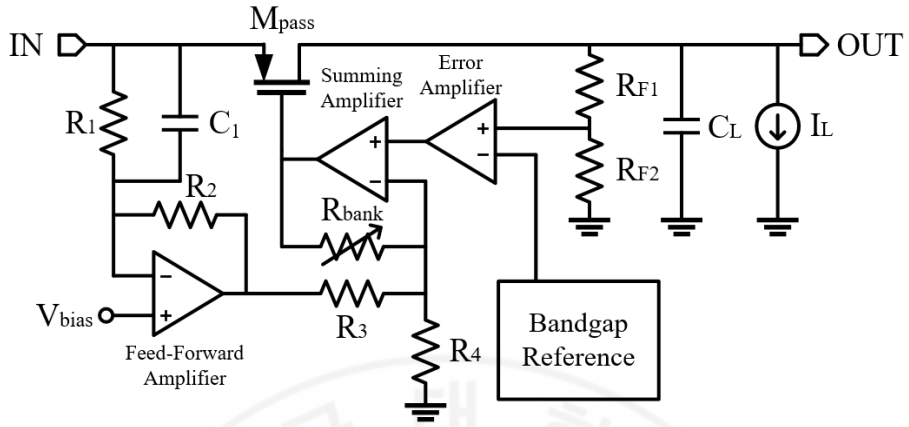

Figure 3.5-1 The schematic diagram of the FFRC LDO.

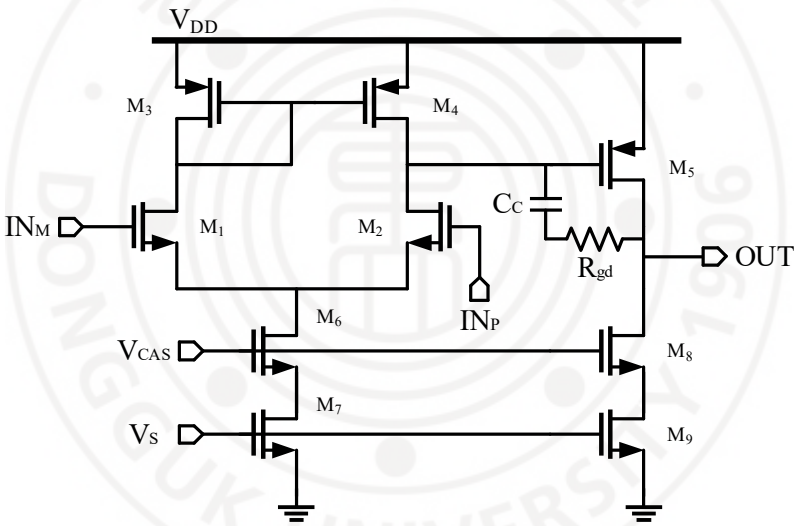

Figure 3.5-2 Transistor-level schematic of feed-forward, summing, and error amplifier.

Table 3.5-1 Parameters of the three amplifiers.

	Feed-Forward Amp	Summing Amp	Error Amp
M_1 [μm/μm]	10/1	10/1	5/1
M_2 [μm/μm]	10/1	10/1	5/1
M_3 [μm/μm]	25/1	25/1	15/1
M_4 [μm/μm]	25/1	25/1	15/1
M_5 [μm/μm]	27/1	50/1	95/1
M_6 [μm/μm]	12/1	8/1	6/1
M_7 [μm/μm]	12/1	-	6/1
M_8 [μm/μm]	12/1	12/1	26/1
M_9 [μm/μm]	12/1	12/1	26/1

C_C [pF]	4	4	1
R_{gd} [kΩ]	4	5	-

Figure 3.5-1 is the schematic diagram of the FFRC LDO [3]. Figure 3.5-2 shows the transistor-level schematic diagram of feed-forward, summing, and error amplifier implemented in the FFRC LDO. Table 3.5-1 shows the parameters of the components in Figure 3.5-2.

To have a clean output voltage, a zero-transfer gain from the input to the output is required. To get the zero-transfer gain in an ideal case, a feed-forward ripple cancellation technique is used in the proposed LDO. A feed-forward path carries the same input ripples through the feed-forward amplifier and the summing amplifier to the gate of the M_{pass}. Then, the ripples at the gate cancels out the ripples at the source of the M_{pass}. However, in the practical case, some of the ripples at the source leak through the drain-source resistance ($r_{ds,pass}$) of the M_{pass}. So, to cancel out the additional ripples from $r_{ds,pass}$, the produced ripples at the gate of the M_{pass} should be higher in ripple amplitude [3].

The pass transistor (M_{pass}) is implemented using a PMOS transistor. PMOS transistor is selected because the DC voltage level needed at the gate is lower than the supply voltage, VDD. While NMOS pass transistor needs a higher DC voltage level at the gate. The length of the pass transistor is 0.1um while the width is 1.5mm.

The error amplifier is implemented to have a feedback circuit and controls the output voltage with R_{F1} and R_{F2}. The summing amplifier's job is to combine the signal from the feed-forward path with the feedback regulating loop. The summing feedback resistances (R_3, R_4, R_{bank}) push the output pole higher so that it is higher than the gain bandwidth (GBW) of the LDO [3].

The operational transconductance amplifier (OTA) consists of a differential amplifier with active load, common source amplifier, compensating capacitor, and a series resistor next to the compensating capacitor. The differential amplifier with active load performs differential to single-ended conversion while maintaining the gain. The capacitor C_C for compensation achieves pole splitting in the circuit, which will affect the stability. Then, the series resistor, R_{gd}, is for providing a left half plane zero to compensate the right half plane zero that was produced by C_C.

To supply a fixed reference voltage to the error amplifier in any conditions like temperature changes or power supply variations, the circuit needs a bandgap voltage reference shown in Figure 3.5-3. The OTA in the bandgap voltage reference is detailly shown in Figure 3.5-4. An OTA is implemented to provide feedback for M_{B1} and M_{B2}. The feedback on the M_{B1} side is implemented as a positive feedback and the other side as a negative feedback. To stabilize the output voltage of the bandgap reference is to have more negative feedback than the positive one. Three resistors R_{B1}, R_{B2}, and R_{B3} make the negative feedback stronger than the positive feedback. The reference voltage (V_{REF}) of 880mV was selected to have 1V on the output voltage. The resistors R_{F1} and R_{F2} determines the output voltage, 1V, based on the ratio of those resistors and the reference voltage from the bandgap reference. The equation for the output voltage (V_{output}) can be expressed as equation 3.5-1.

$$V_{OUTPUT}[V] = V_{REF} \times \frac{R_{F1} + R_{F2}}{R_{F2}}[V] \qquad (3.5\text{-}1)$$

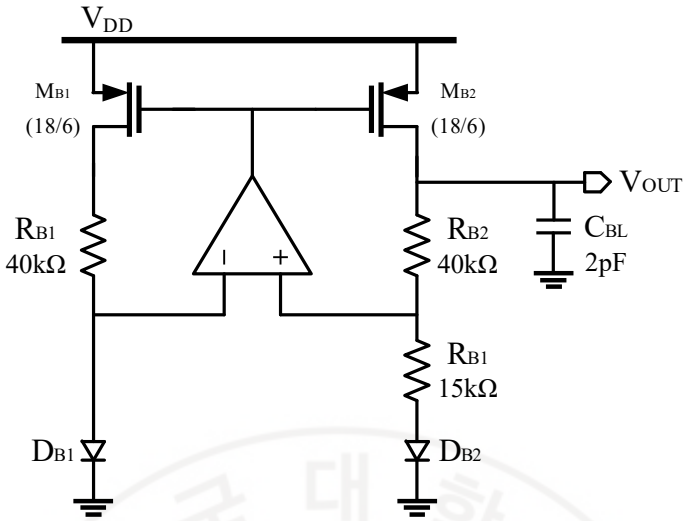

Figure 3.5-3 Schematic diagram of the bandgap voltage reference.

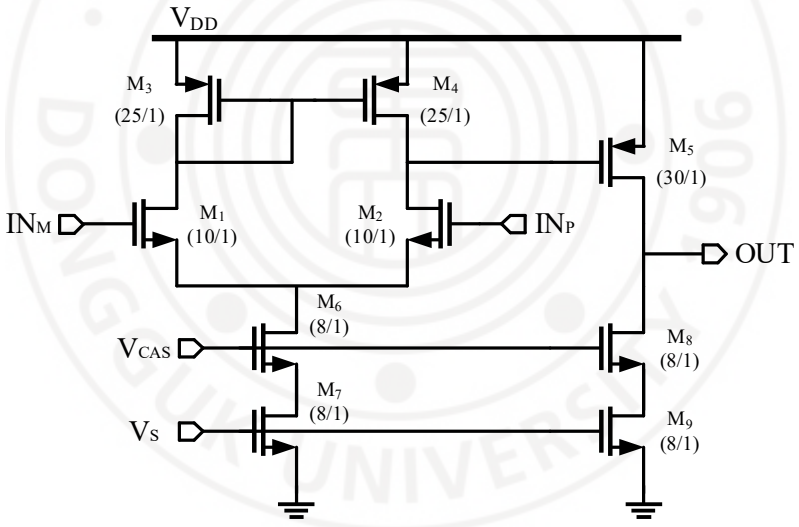

Figure 3.5-4 OTA schematic diagram of the bandgap voltage reference.

For the resistor bank (R_{bank}), it is designed so that it has a range of resistance from 750Ω to 1125Ω. This is because the 65-nm CMOS process that was used had an error range of 20%. The aimed resistance of the resistor bank is about 950Ω.

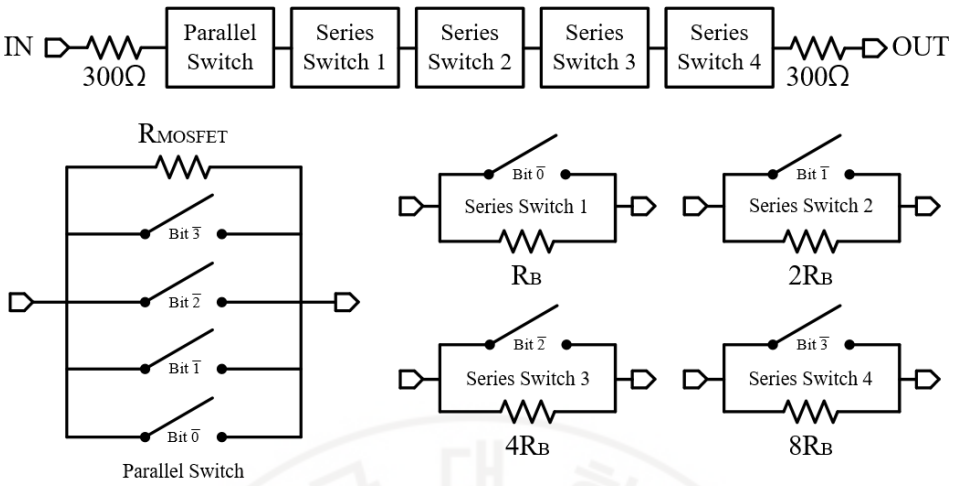

Figure 3.5-5 Diagram of the resistor bank.

Figure 3.5-5 shows the diagram of the resistor bank in the FFRC LDO. The parallel switch and the series switches use bits 0, 1, 2, and 3. The fifteen resistors, R_B, are there to have a 25Ω step from 750Ω to 1125Ω. The fifteen resistors, R_B, are there to have a 25Ω step from 750Ω to 1125Ω. The parallel switches make the entire resistance fixed so that only the number of R_B determines the total resistance. The equation for the resistor bank is given by equation 3.5-2.

$$R_{bank}[\Omega] = 600 + \frac{R_{MOSFET}R_P}{R_P + (b_0 + b_1 + b_2 + b_3)R_{MOSFET}} + R_B b_0 + 2R_B b_1 + 4R_B b_2 + 8R_B b_3[\Omega] \quad (3.5\text{-}2)$$

where R_P is the parallel switch and b_{number} is the bit number. The resister bank table is shown in Table 3.5-2.

Table 3.5-2 Bit Table of Resister Bank.

Bit 3	Bit 2	Bit 1	Bit 0	Resistance [Ω]
0	0	0	0	744
0	0	0	1	772
0	0	1	0	796
0	0	1	1	827
0	1	0	0	845
0	1	0	1	876
0	1	1	0	900
0	1	1	1	935
1	0	0	0	951

1	0	0	1	981
1	0	1	0	1,006
1	0	1	1	1,041
1	1	0	0	1,056
1	1	0	1	1,091
1	1	1	0	1,115
1	1	1	1	1,157

Figure 3.5-6 shows the full chip microphotograph of the FFRC LDO.

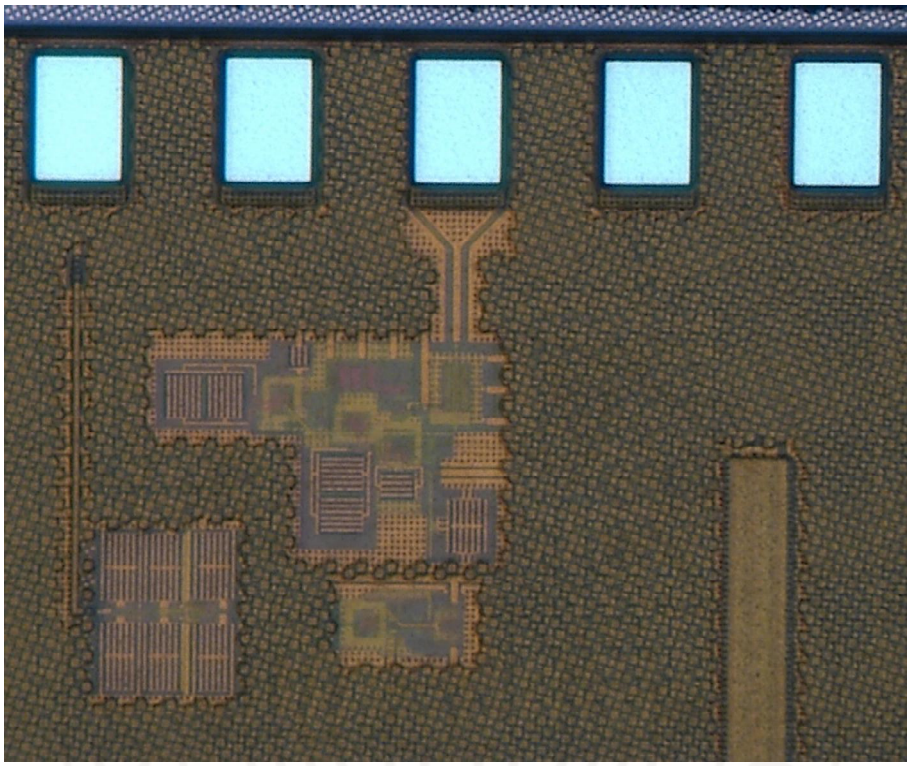

Figure 3.5-6 The full chip microphotograph of the FFRC LDO.

The system layout includes:

(1) Pass Transistor

(2) Feed-forward Amplifier

(3) Error Amplifier

(4) Summing Amplifier

(5) Bandgap reference

(6) Biasing circuit

Chapter 4 POWER AMPLIFIER & LDO MEASUREMENT RESULTS

4.1 Power Amplifier Measurement Results

Figure 4.1-1 and Figure 4.1-2 shows the measurement and probing setup for the proposed 5 GHz power amplifier. Figure 4.1-3 is the power supply rejection ratio measurement setup.

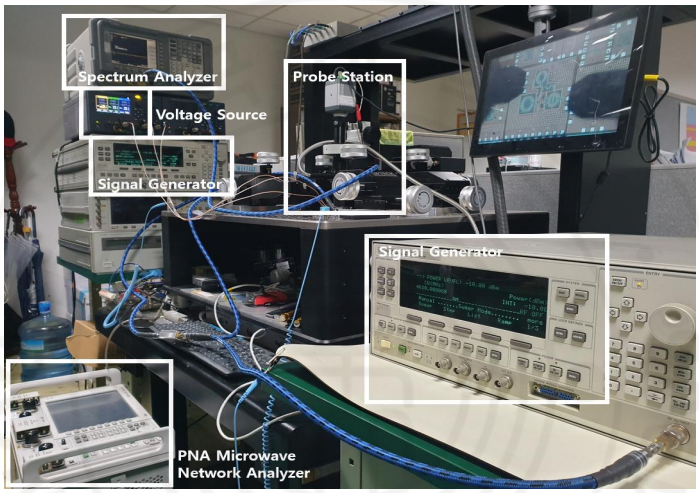

Figure 4.1-1 Measurement setup of the proposed PA.

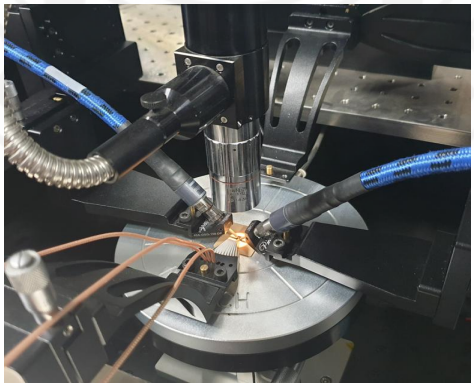

Figure 4.1-2 Probing setup of the proposed PA.

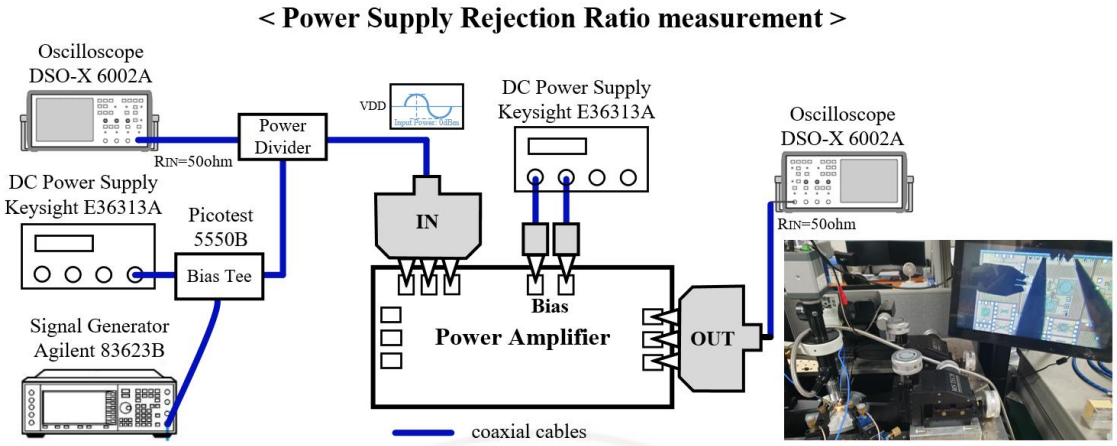

Figure 4.1-3 The PSRR measurement setup.

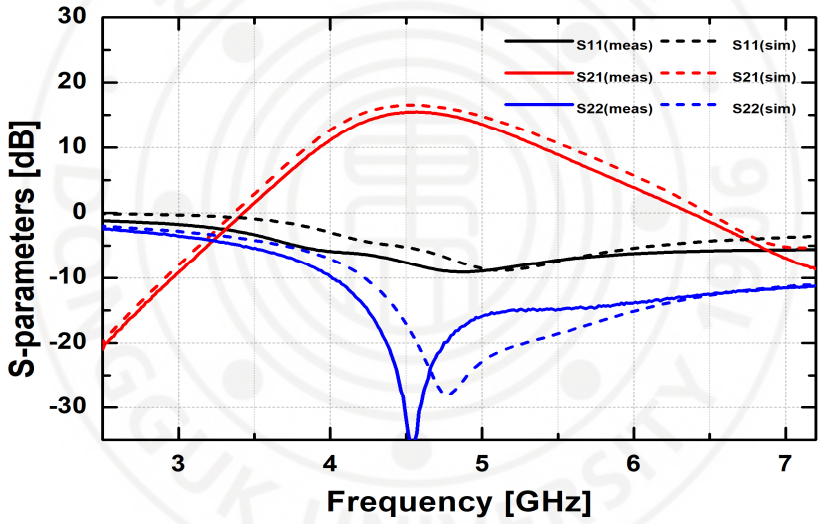

Figure 4.1-4 The simulation and measurement results of S-parameters of the proposed PA.

Figure 4.1-4 shows the simulation and measured S-parameters of the proposed 5GHz power amplifier. The measurement was done with the Keysight N5224A PNA. Under a 1.8V supply voltage, 72mA of current consumption was measured. The maximum value of insertion loss (S21) was 15.5 dB at 4.6 GHz. The 3 dB bandwidth of the implemented PA was 1 GHz (from 4.1 GHz to 5.1 GHz).

Agilent 83623B signal generator and an Agilent E4405B spectrum analyzer were used to measure the power added efficiency (PAE), the output-referred 1 dB compression point (OP1dB), and the output-referred third-order intercept point (OIP3). Figure 4.1-5 shows that the OP1dB is 13dBm, saturated power is 15.4 dBm, and the peak PAE is 15%. Figure 4.1-6 represents the measured output signal when intermodulation was performed with a frequency offset of 5 MHz. As can be seen, Figure 4.1-6 and Figure 4.1-7 shows that the measured OIP3 is 22 dBm when the IIP3 is 6.5 dBm.

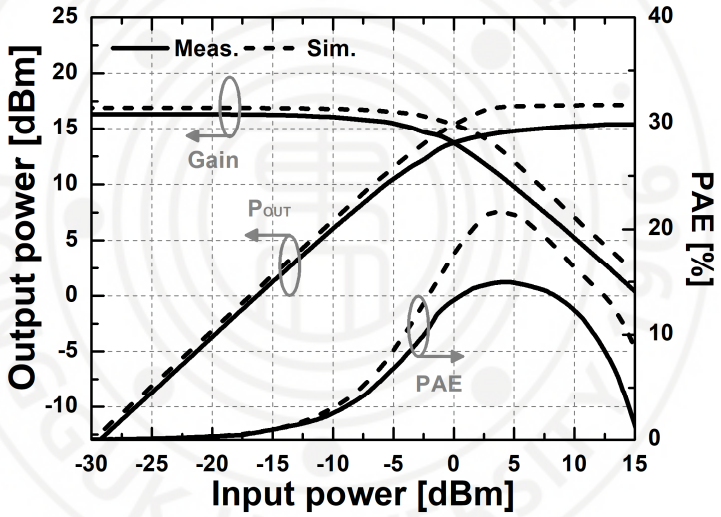

Figure 4.1-5 The simulation and measurement results of gain, POUT, and power-added efficiency (PAE) of the implemented PA.

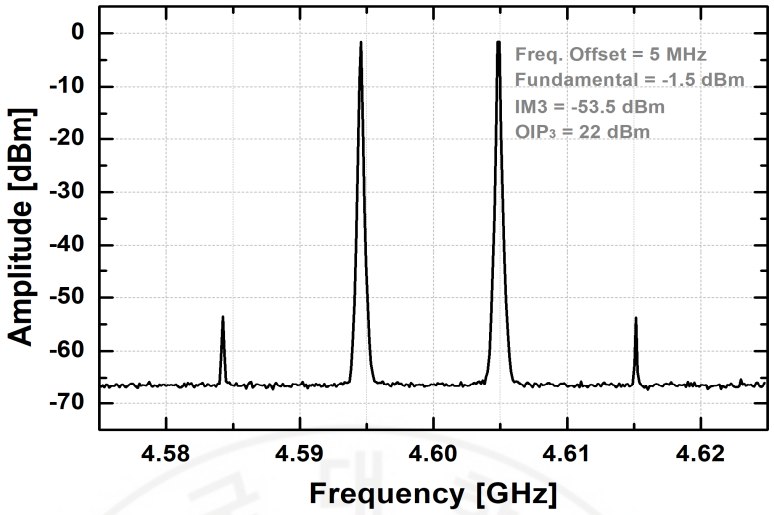

Figure 4.1-6 The output signal of the proposed PA.

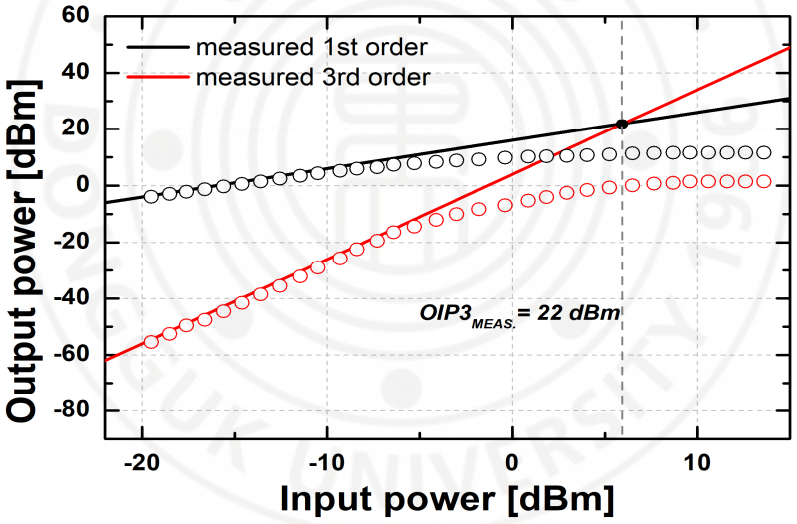

Figure 4.1-7 The measurement of the output-referred third-order intercept point (OIP3) of the proposed two-stage PA.

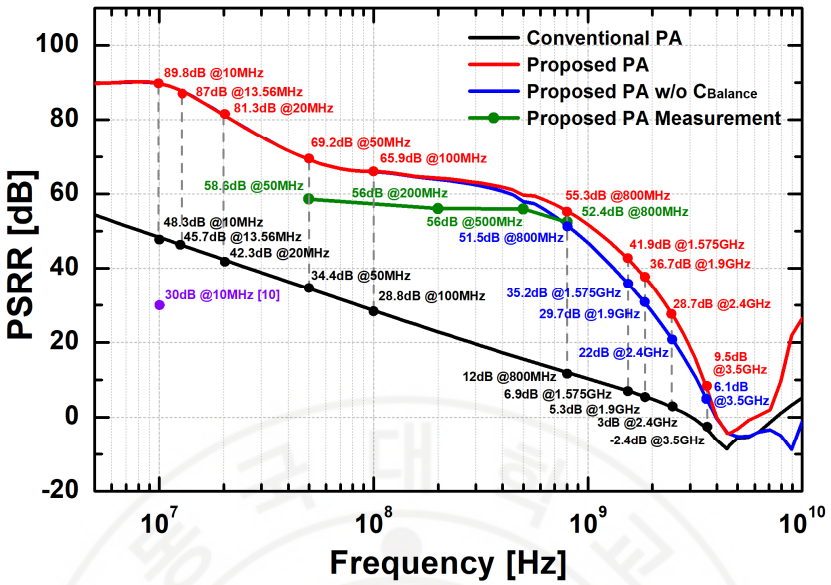

Figure 4.1-8 The simulated power supply rejection ratio (PSRR) of the proposed PA (excluding $C_{Balance}$), a conventional PA, and the simulated and measured PSRR of the proposed PA, with the reference [18]'s reported PSRR.

Figure 4.1-8 shows the simulated power supply rejection ratio (PSRR) of the proposed PA (excluding $C_{Balance}$), a conventional PA, and the simulated and measured PSRR of the proposed PA. Table 4.1-1 compare between our work and previously published PAs. The figure of merit (FoM) is given by

$$FoM = \frac{P_{RFout} \times PAE \times OIP3 \times f^2}{Area} [dBm \cdot GHz^2/mm^2] \qquad (4.1\text{-}1)$$

where P_{RFout} is the output RF power and Area is the chip occupation size. The FoM of this design is 45 $(dBm \cdot GHz^2)/mm^2$, which demonstrates a comparable power amplifier performance while achieving a substantially improved PSRR at the frequencies used for many different wireless communications [13].

Table 4.1-1 Comparison of the power amplifiers.

PA	This Work	[4]	[7]	[18]	[19]	[20]	[21]	[22]	[23]
Technology [nm]	180	180	55	350	180	180	180	180	180
Frequency [GHz]	4.1–5.1	2.4	2.4	10.6 MHz	2.4	5.8	5	5	2.5
Supply Voltage [V]	1.8	1.8	3.3	3	1.8	1.8	1.8	1.8	1
P_{SAT} [dBm]	15.4	15	29	-	5	26.7	17.4	24.1	10.1
PAE(1) [%]	15	-	-	-	20	19	27.1	13	34.5
OP1dB [dBm]	13	-	27.5	-	4	24.2	15.4	21.8	8
OIP3(2) [dBm]	22	-	-15	-	15	-	25	-	-
PSRR [dB at 10MHz]	82.5	25	-	30	-	-	-	-	-
Area [mm^2]	0.65	1.96	6.6	-	0.8	1.92	.84	1.8	-
FoM* [$(dBm \cdot GHz^2)/mm^2$]	45	-	-	-	21.6	-	51.5	-	-

(1) $PAE = \frac{P_{RFout} - P_{RFin}}{P_{diss}} \times 100\%$, (2) $OIP3 = IIP3_{(3)} + Gain$, (3) $IIP3 = P_{RFout} + \frac{IMD}{2} - Gain$

4.2 Comparison between Conventional LDO and FFRC LDO

The feed-forward ripple cancellation (FFRC) low dropout regulator provides more than 40 dB of PSRR compared to a conventional LDO at 10MHz.

4.2.1 Power Supply Rejection Ratio Measurement

Figure 4.2-1 shows the PSRR measurement setup of LDO [3]. The VDD of the LDO is provided by E36313A power supply, while 83623B signal generator provides the artificially generated ripple through the 5550B bias tee. By using the DSO-X 6002A oscilloscope, the input and output signal is measured to get the PSRR. The graph of PSRR changes if the load resistor changes.

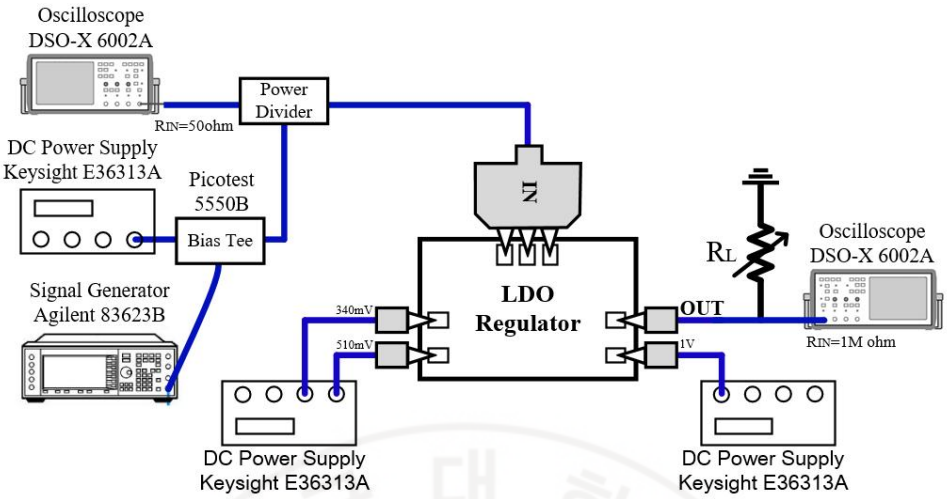

Figure 4.2-1 The PSRR measurement setup.

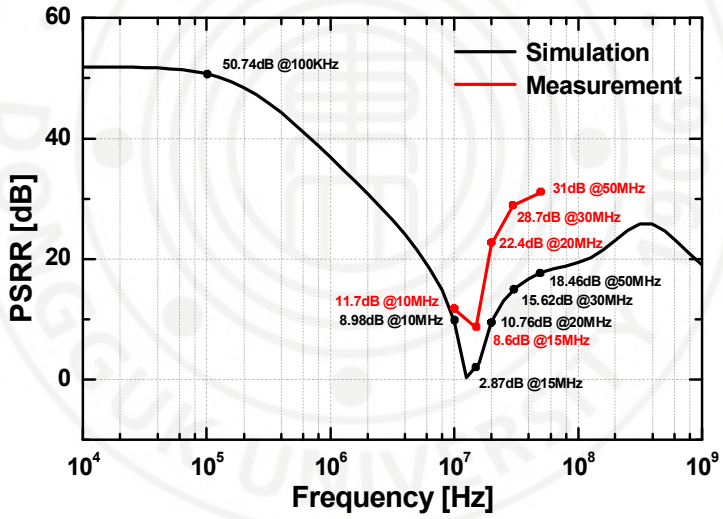

Figure 4.2-2 The simulation and measurement of PSRR in the conventional LDO regulator.

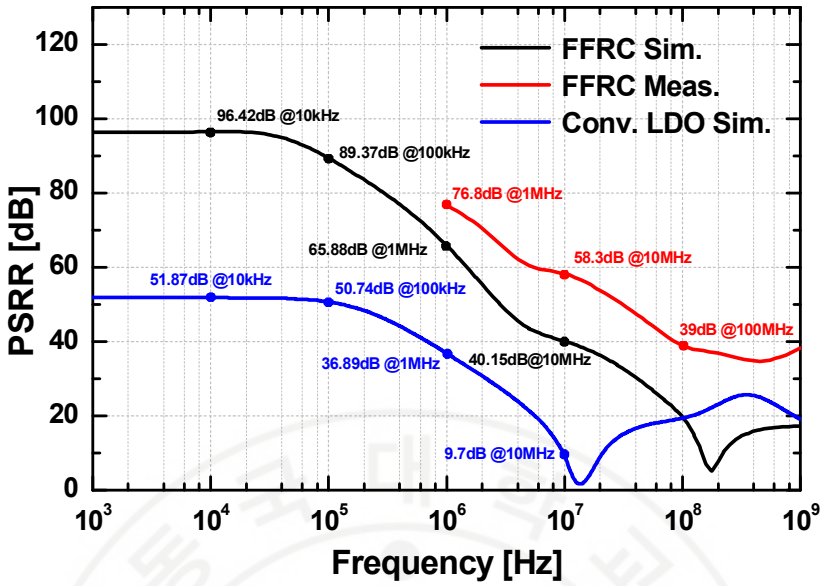

Figure 4.2-3 The simulation of PSRR in the FFRC LDO regulator.

Figure 4.2-2 shows the simulated and measured load regulation results of the conventional LDO regulator. Figure 4.2-3 shows the simulated load regulation results of the FFRC LDO regulator.

4.2.2 Load/Line Regulation Measurement

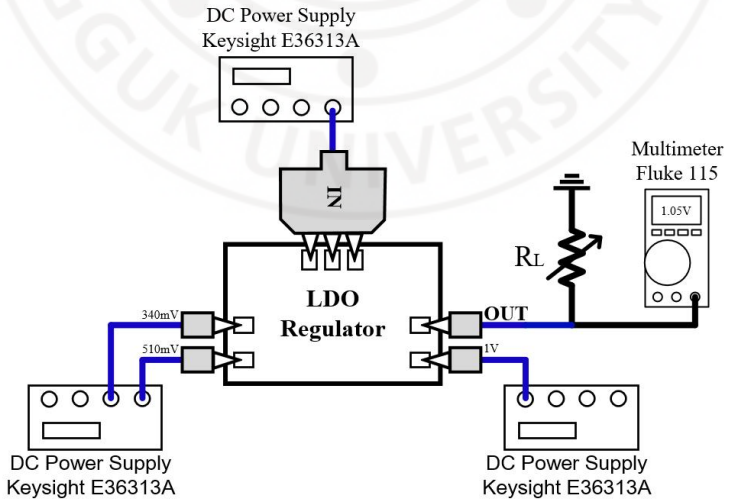

Figure 4.2-4 The load/line regulation measurement setup.

Figure 4.2-4 shows the load and line regulation measurement setup of LDO [3]. To measure load regulation, the input voltage is fixed, and the load resistor must change. By measuring the load resistance and regulated output voltage, load current is calculated.

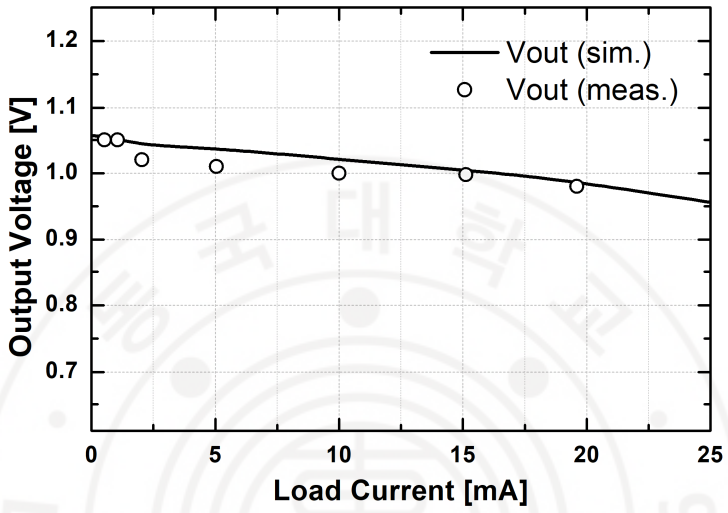

Figure 4.2-5 The simulation and measurement of load regulation in the conventional LDO regulator.

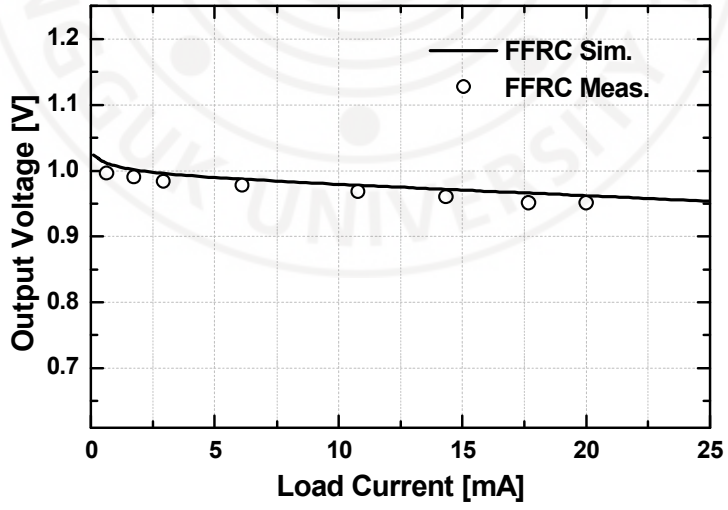

Figure 4.2-6 The simulation of load regulation in the FFRC LDO regulator.

The simulated and measured load regulation results of the conventional LDO regulator is shown in figure 4.2-5. The simulated load regulation results of the FFRC LDO is shown in Figure 4.2-6.

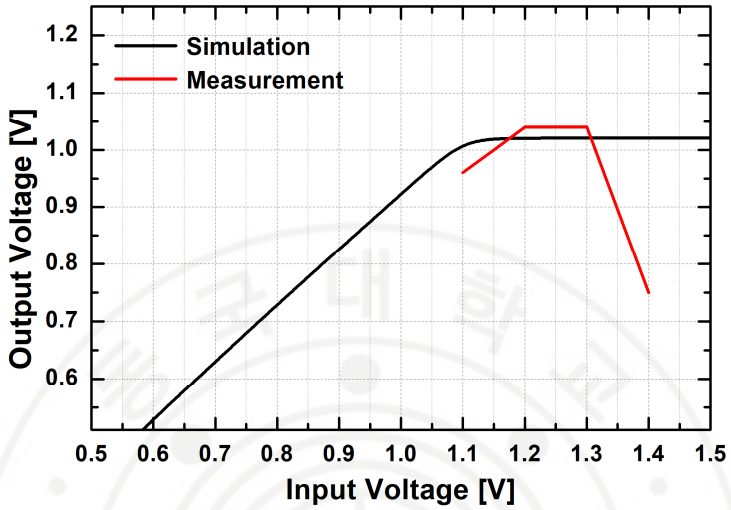

Figure 4.2-7 The simulation and measurement of line regulation in the conventional LDO regulator with load resistance of 100 Ohm.

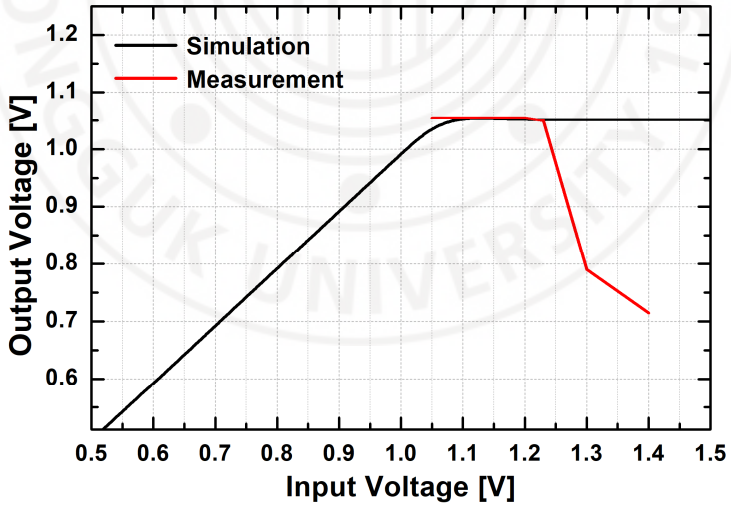

Figure 4.2-8 The simulation and measurement of line regulation in the conventional LDO regulator with load resistance of 1K Ohm.

Figure 4.2-7 and Figure 4.2-8 shows the simulated and measured line regulation results with 100 Ohm and 1K Ohm load resistance in the conventional LDO regulator. Figure 4.2-9 is the simulated line regulation results with 100 Ohm load resistance of the FFRC LDO. Table 4.2-1 shows the comparison table of published papers and this work.

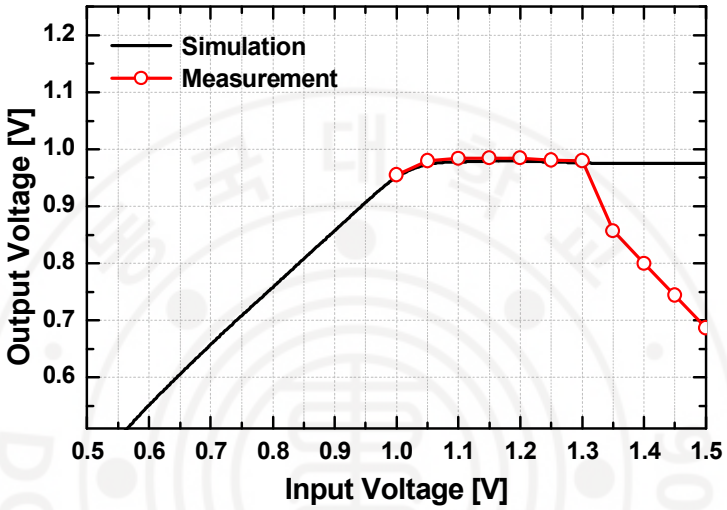

Figure 4.2-9 The simulation of line regulation in the FFRC LDO regulator with load resistance of 100 Ohm.

Table 4.2-1 Comparison of LDOs.

LDO	This Work	[27]	[28]	[29]
Technology [nm]	65	180	180	350
V_{IN} [V]	1.2	-	1.5	3.7-5.2
V_{OUT} [V]	0.98	-	1	3-3.6
Dropout Voltage [V]	0.22	0.3	0.5	0.3
Maximum Load [mA]	20	4	100	100
Quiescent Current [μA]	385	28	145	-
PSRR [dB]	76.8@1MHz 58.3@10MHz	37@1MHz <20@10MHz	~30@1MHz <0@10MHz	25@3MHz
Load Regulation [mV/mA]	2.3	0.175	0.012	-
Line Regulation [mV/mV]	0.05	0.024	0.37	-
Area [mm^2]	0.092	0.105	-	0.452

Chapter 5 CONCLUSION

In this dissertation, a compact 5 GHz class-A power amplifier applicable for a wireless combo-chip that supports multiple radio systems in 180-nm CMOS process is proposed, as well as a feed-forward ripple cancellation low dropout regulator which generate a wide bandwidth of high PSRR. The transformer-based balun in the 5 GHz power amplifier made a differential structure which improved PSR significantly. Then another transformer-based balun combined the differential signal to drive a single-ended 50 Ohm load. The proposed power amplifier was able to achieve 9.5 dB to 65.9 dB of PSRR at 0.1~3.5 GHz. The power amplifier also has a gain of 15.5 dB, an OP1dB of 13 dBm, an OIP3 of 22 dBm with a 5 MHz frequency offset, an output saturated power of 15.4 dBm, and a peak PAE of 15%. The feed-forward ripple cancellation (FFRC) low dropout regulator provides more than 40 dB of PSRR compared to a conventional LDO at 10MHz.

For future research, I plan to research more on improving the linearity and efficiency of the power amplifier. I think it is possible to improve more on the OIP3 and PAE. The PAE, compared to other published literature, should be higher.

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